

Enrico/Caruso 15" UMA Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2011-04-22

REV : A00

DY : Nopop Component
HDMI : Pop for HDMI function
No_HDMI : Pop for NO HDMI function
10/100 : Pop for 10/100 LAN
GIGA : Pop for GIGA LAN
Surge : Pop for surge option
G709 : Pop G709 thermal solution
INS : Pop for Inspiron series ID
VOS : Pop for Vostro series ID
S3 : Pop for S3 power reduction
Normal : Pop for NO S3 power reduction

DV15 CP UMA second



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Title

Cover Page

Size
A3

Document Number

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Rev

A00

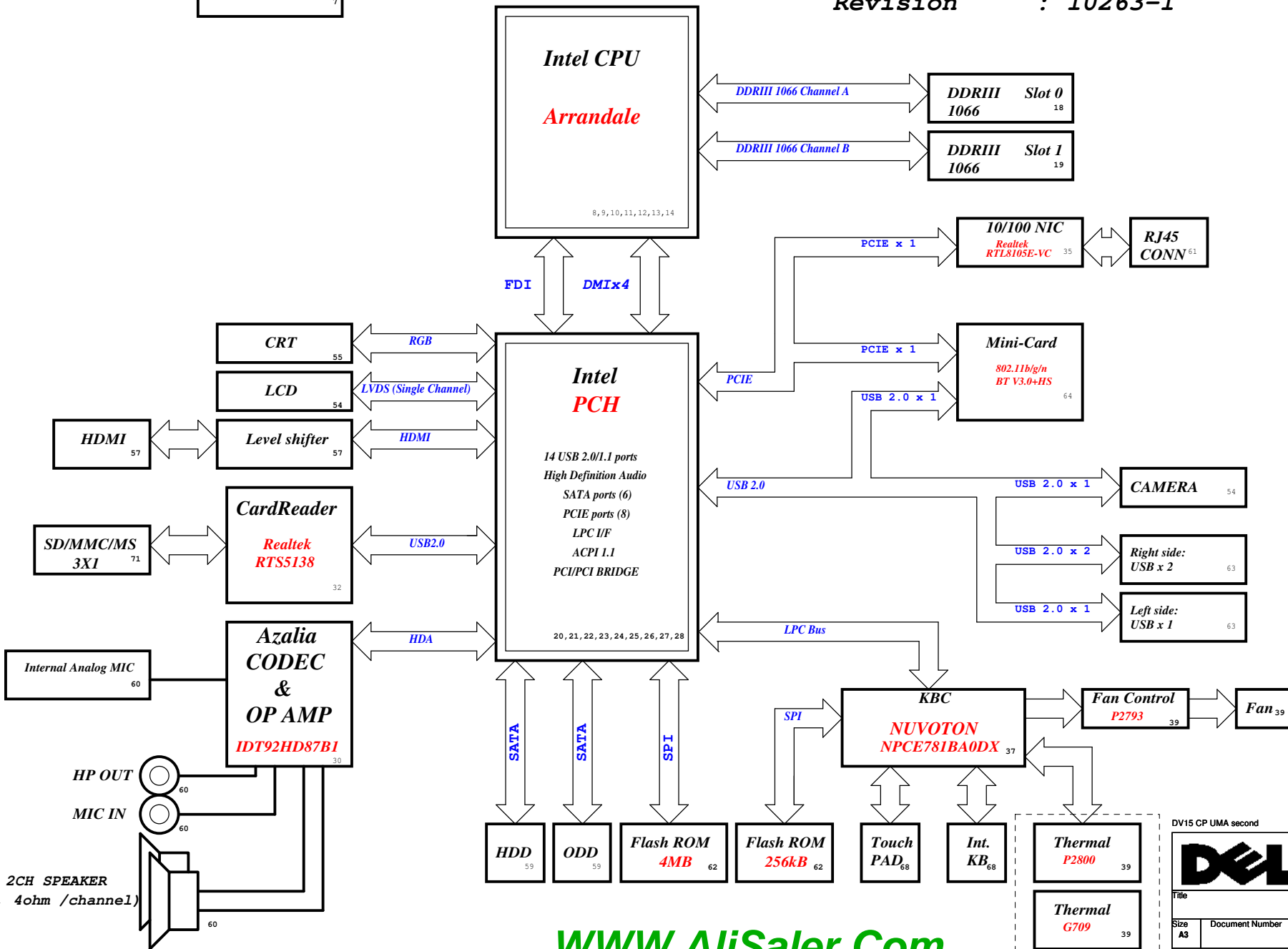
Date: Friday, April 22, 2011

Sheet 1 of 99

DV15 Calpella UMA Block Diagram

Project code : 91.4IP01.001
PCB P/N : 48.4IP01.011
Revision : 10263-1

Clock Generator
SLG8SP595



MAXIM CHARGER	
BQ24707 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
TPS51123 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +3.3V_ALW +5V_ALW +15V_ALW
CPU DC/DC	
ISL62882 47, 48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
RT8237A 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_CPU +1.05V_PCH
SYSTEM DC/DC	
RT8207 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +V_DDR_REF +0.75V_DDR_VTT
SYSTEM DC/DC	
APW7153B 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_CPU +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top L2: GND L3: Signal L4: Signal L5: VCC L6: Bottom	

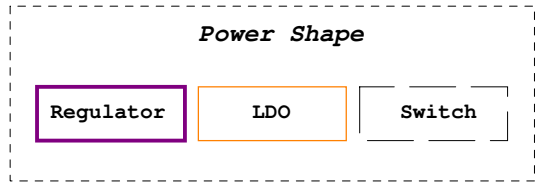
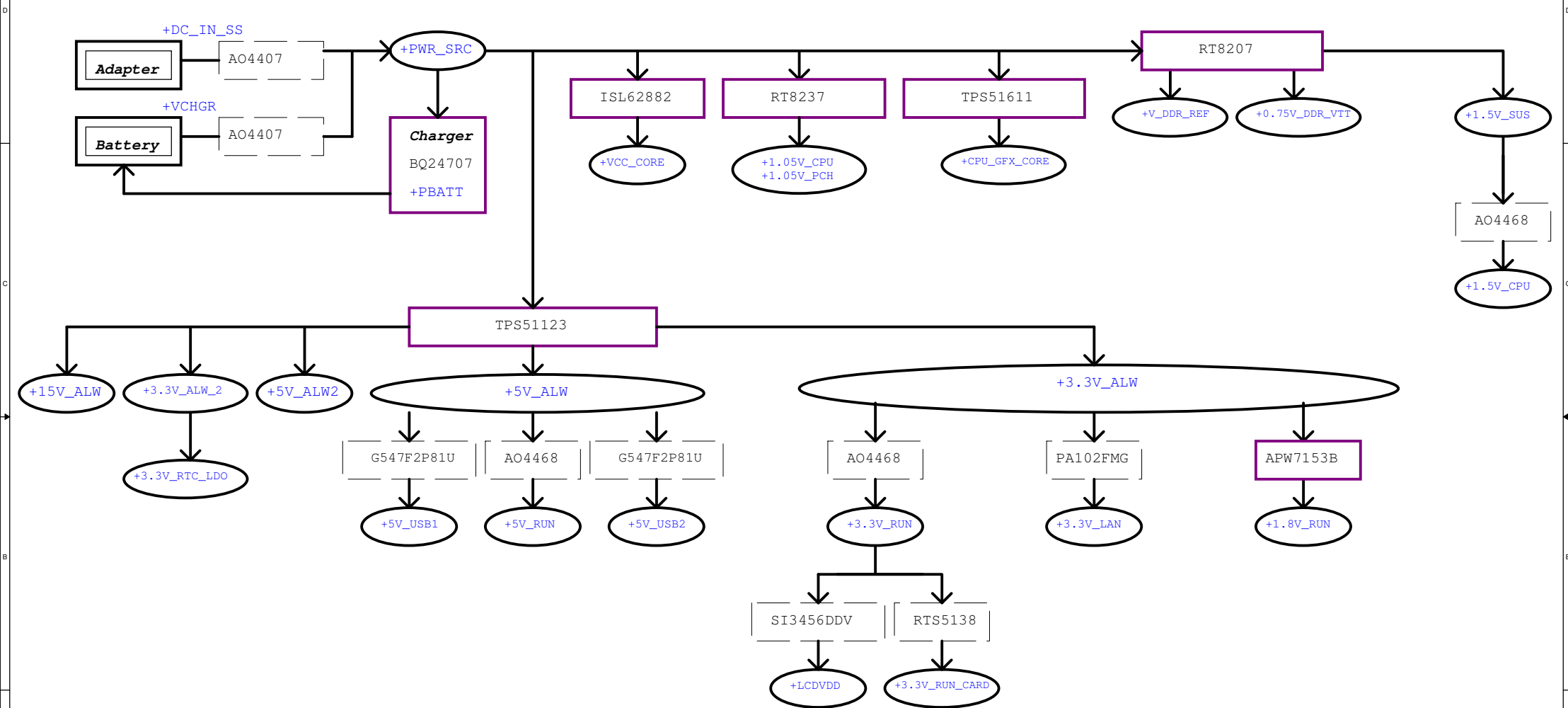
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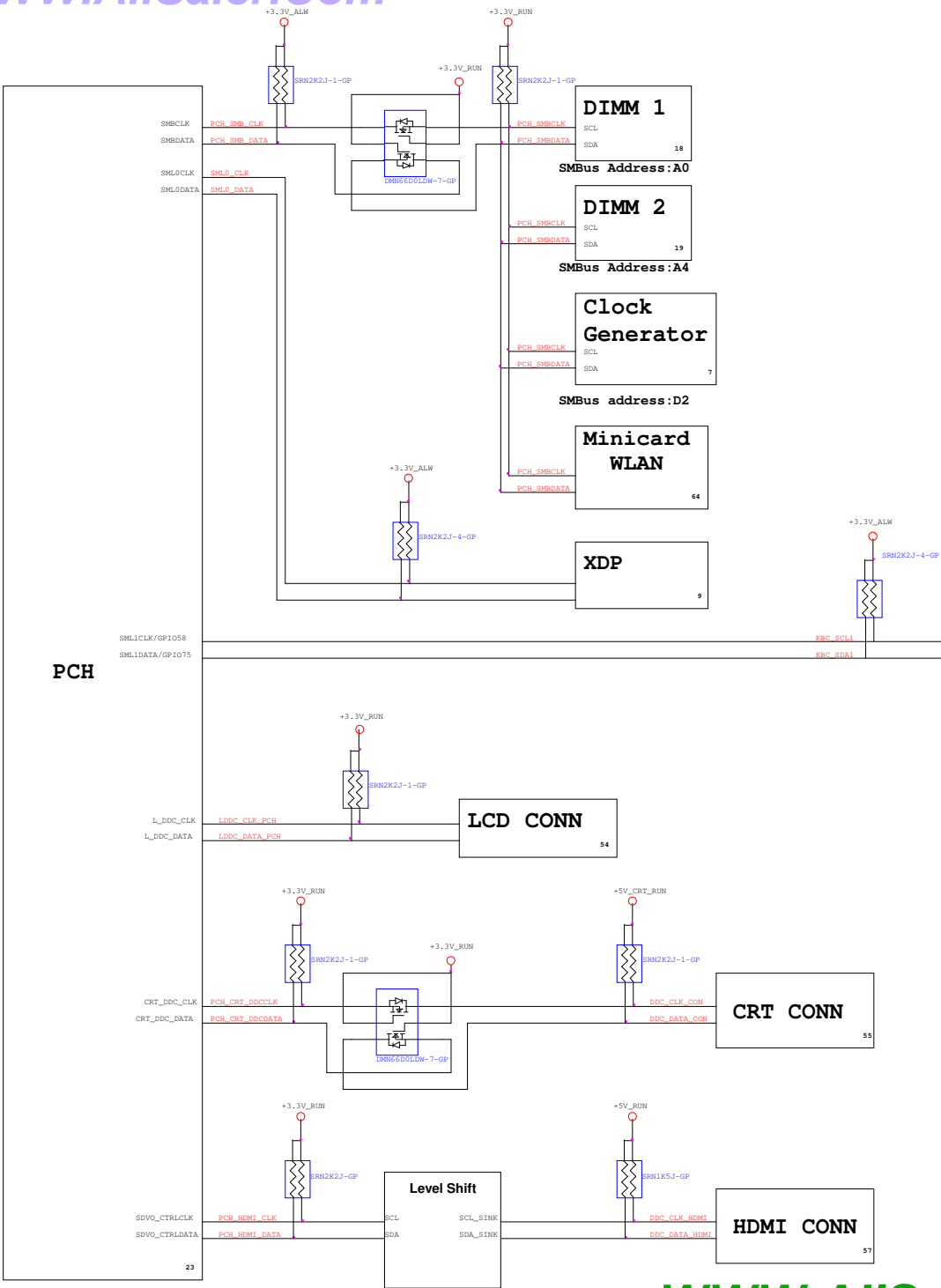
Title: **Block Diagram**

Size: A3 Document Number: **Enrico/Caruso 15 CP** Rev: **A00**

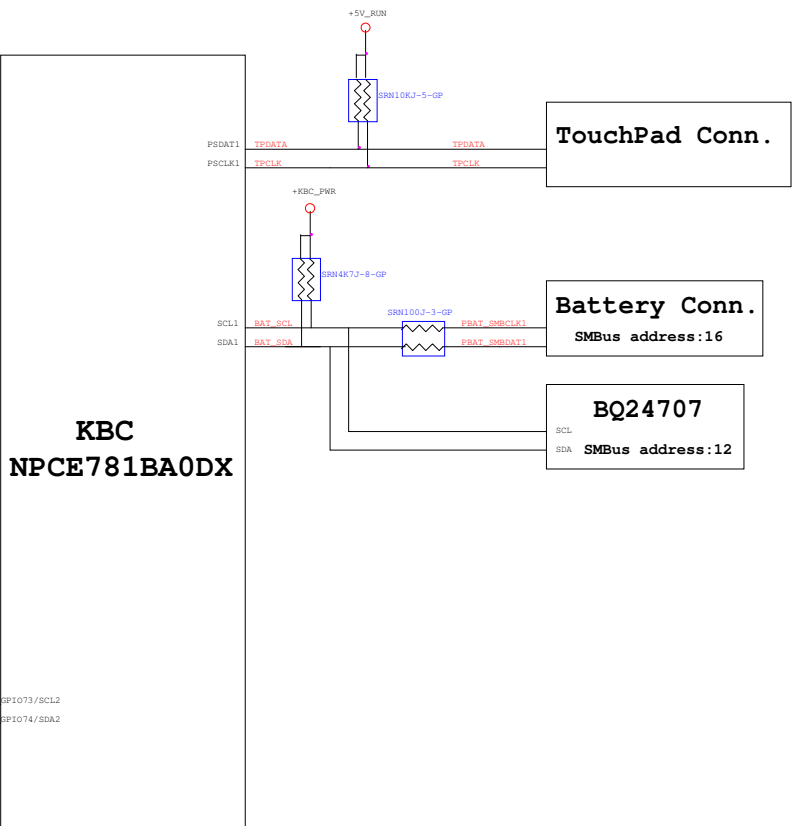
Date: Friday, April 22, 2011 Sheet: 2 of 99



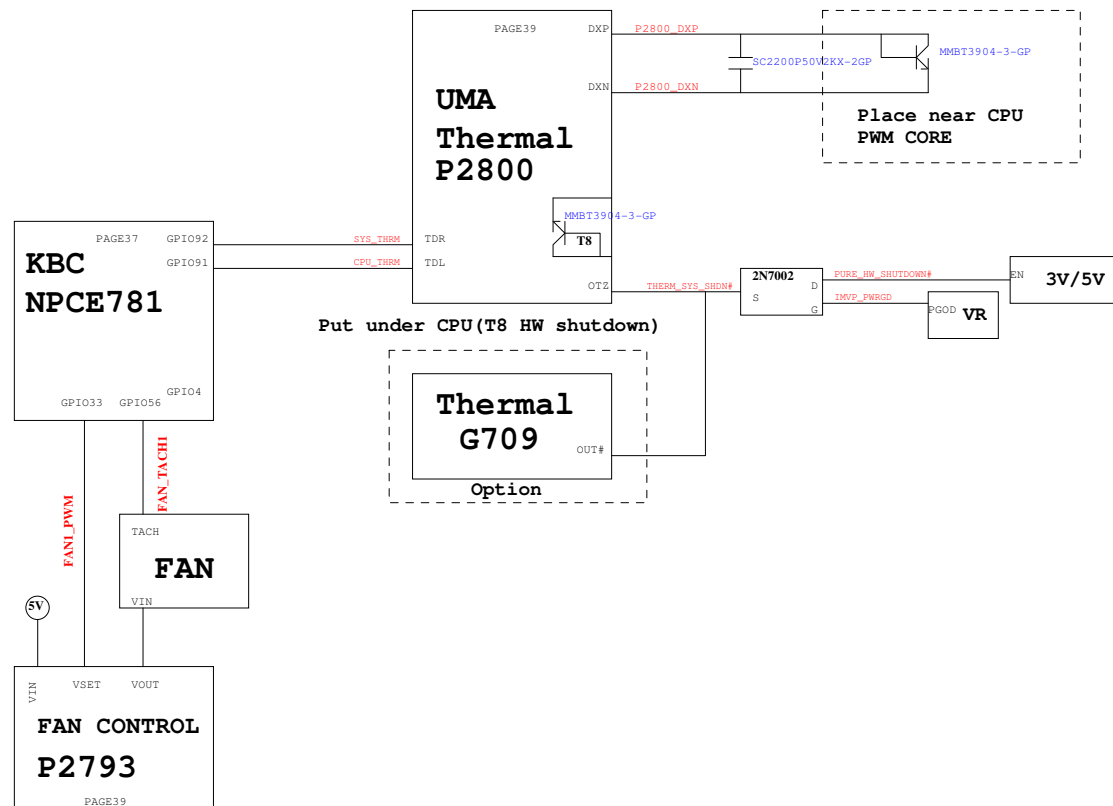
PCH SMBus Block Diagram



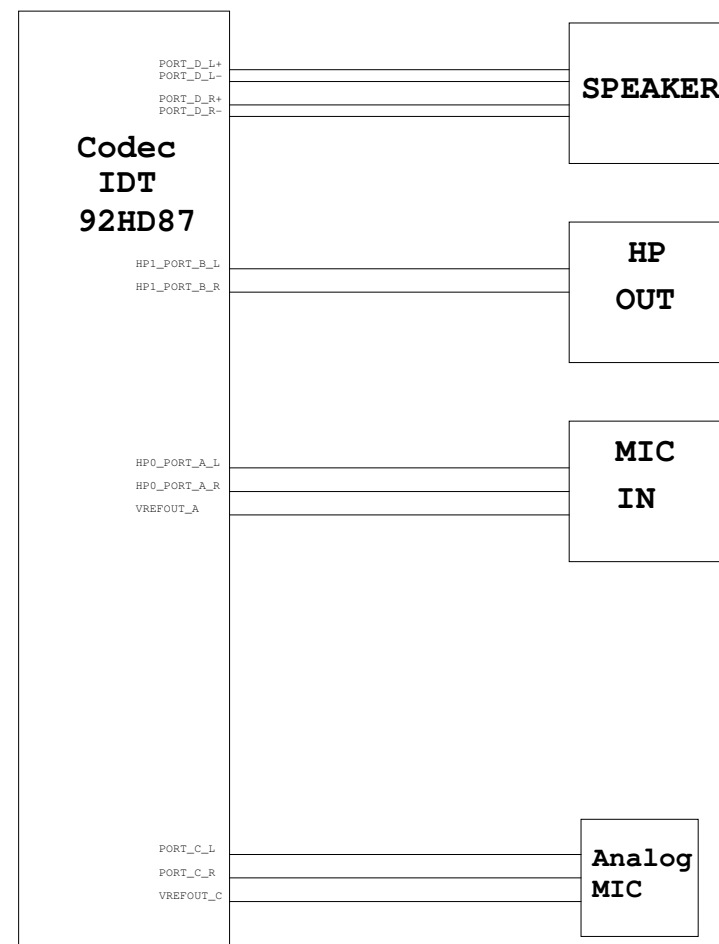
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	X
1	USB1
2	USB2 (Ext I/O BD)
3	USB3 (Ext I/O BD)
4	X
5	X
6	X
7	X
8	X
9	WLAN + Bluetooth
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

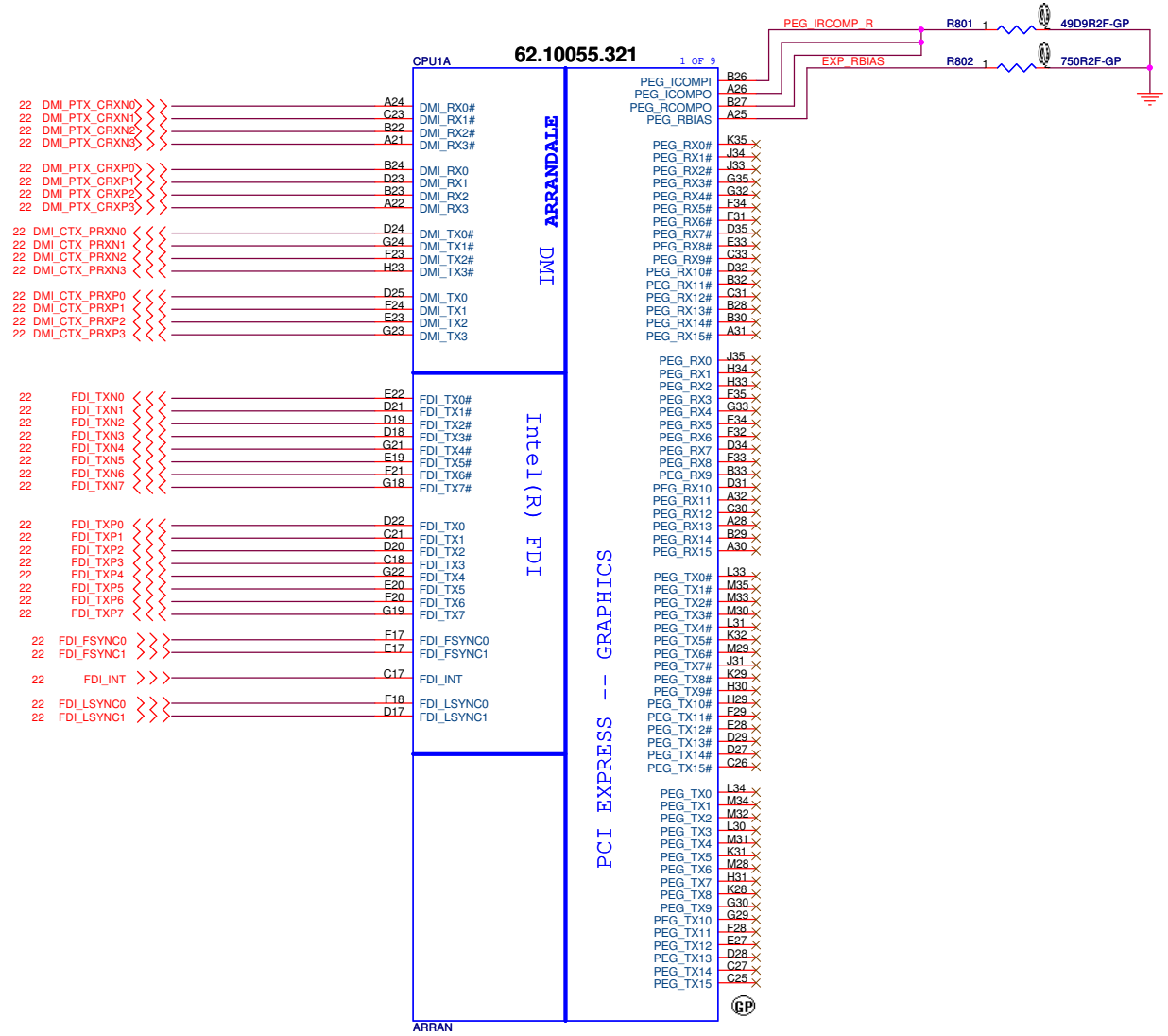
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Title			
<i>Table of Content</i>			
Size A3	Document Number <i>Enrico/Caruso 15 CP</i>		Rev <i>A00</i>
Date: Friday, April 08, 2011	Sheet	6 of	99



SSID = CPU

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Title

CPU (PCIE/DMI/FDI)

Size

Document Number

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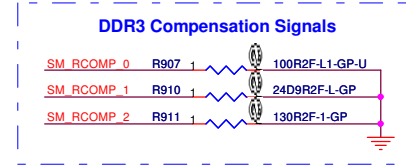
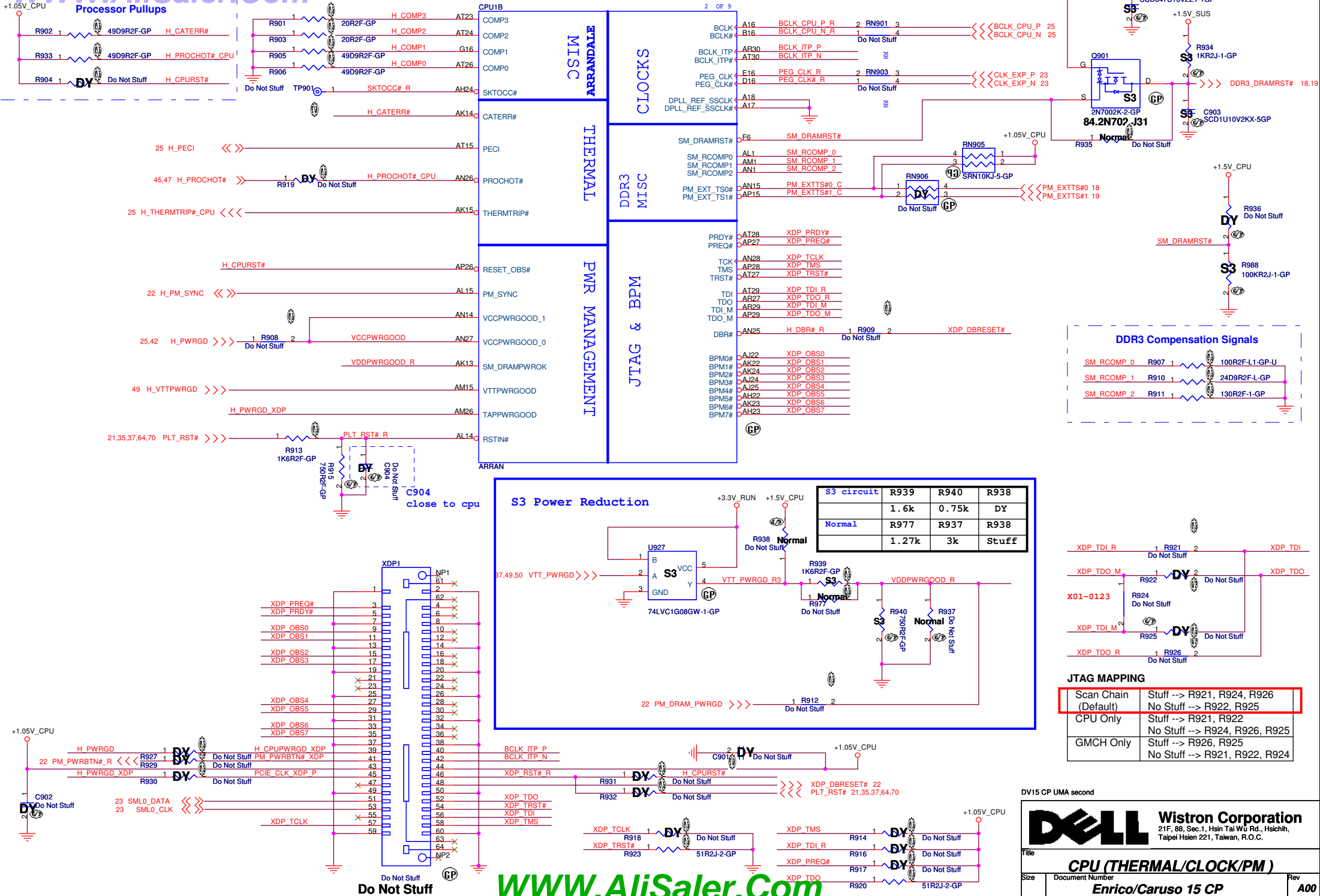
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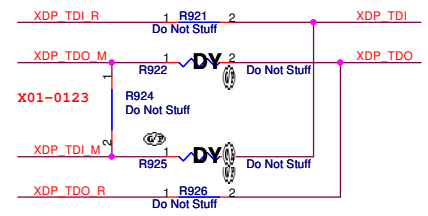
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Sheet 8 of 99

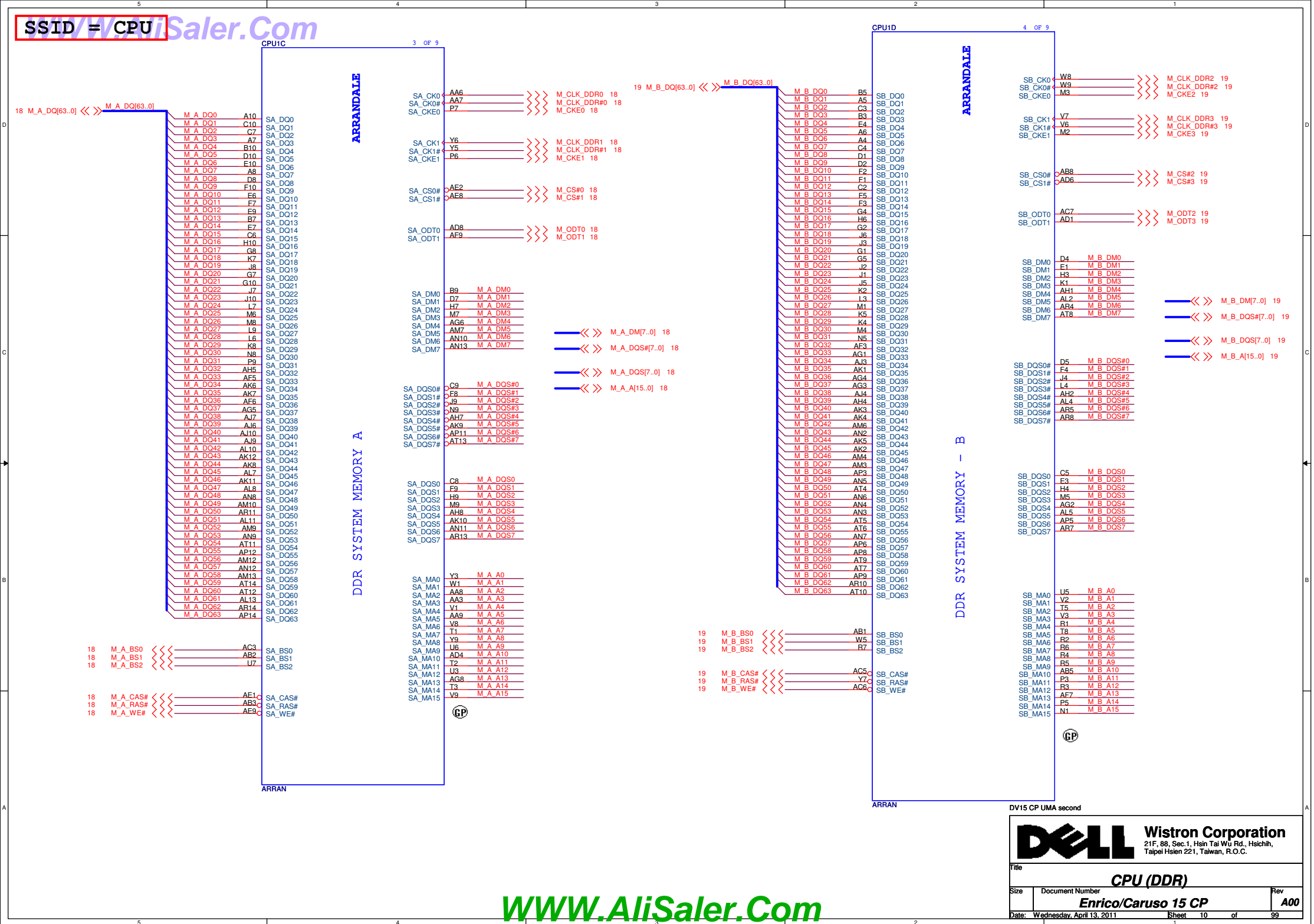
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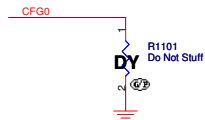


S3 circuit	R939	R940	R938
Normal	1.6k	0.75k	DY
	R977	R937	R938
	1.27k	3k	Stuff

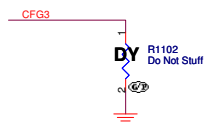


JTAG MAPPING	
Scan Chain (Default)	Stuff --> R921, R924, R926
CPU Only	No Stuff --> R922, R925
GMCH Only	Stuff --> R921, R922
	No Stuff --> R924, R926, R925
	Stuff --> R926, R925
	No Stuff --> R921, R922, R924

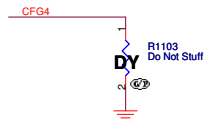




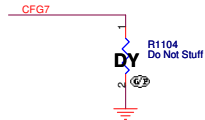
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



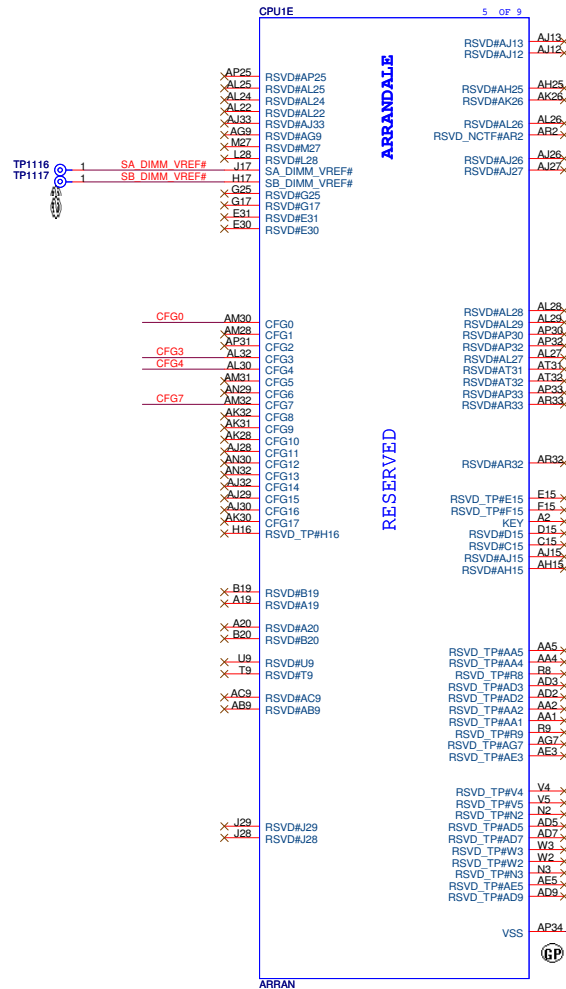
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



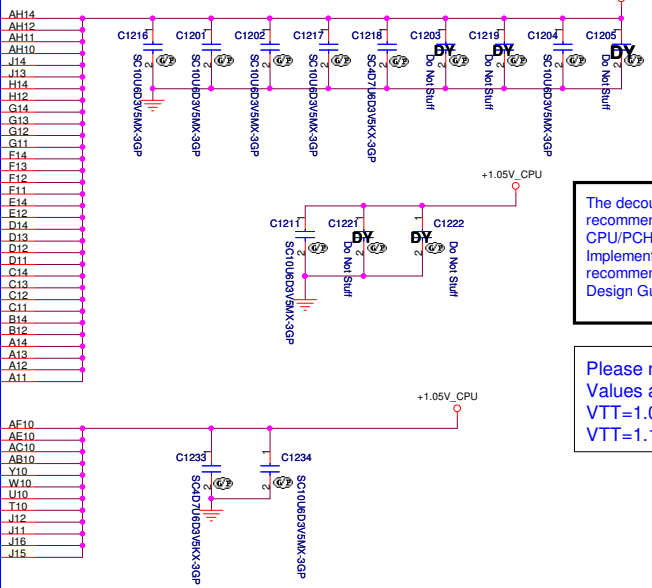
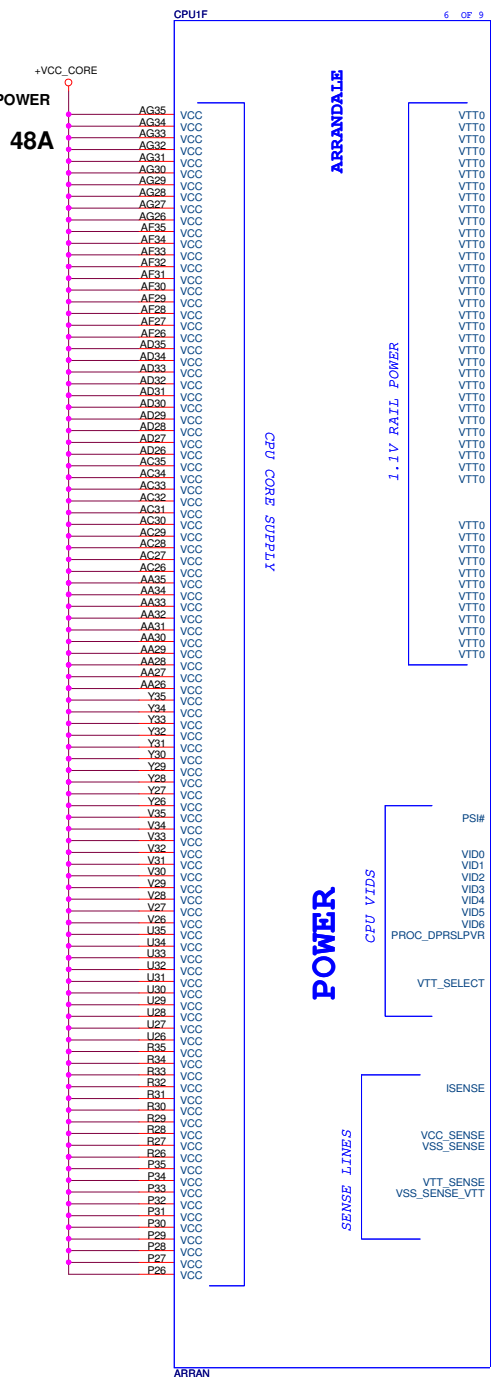
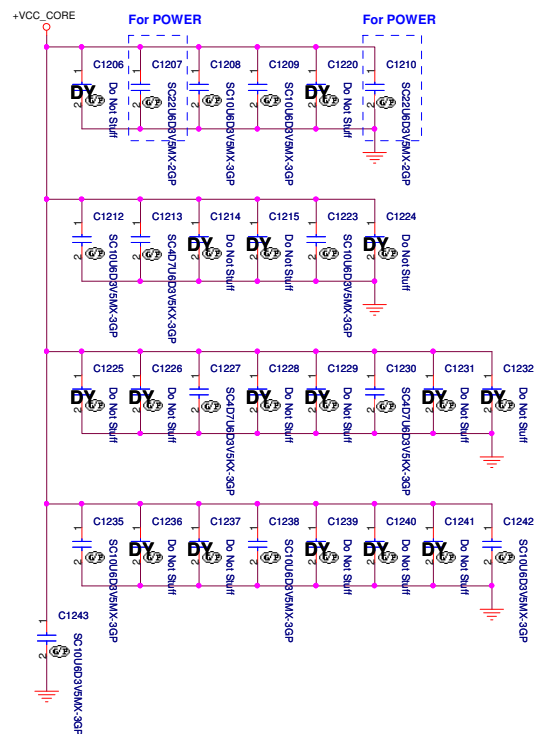
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

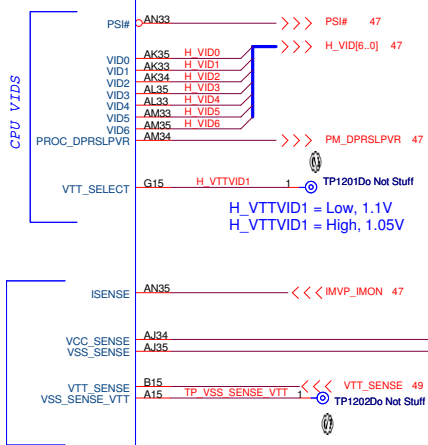


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



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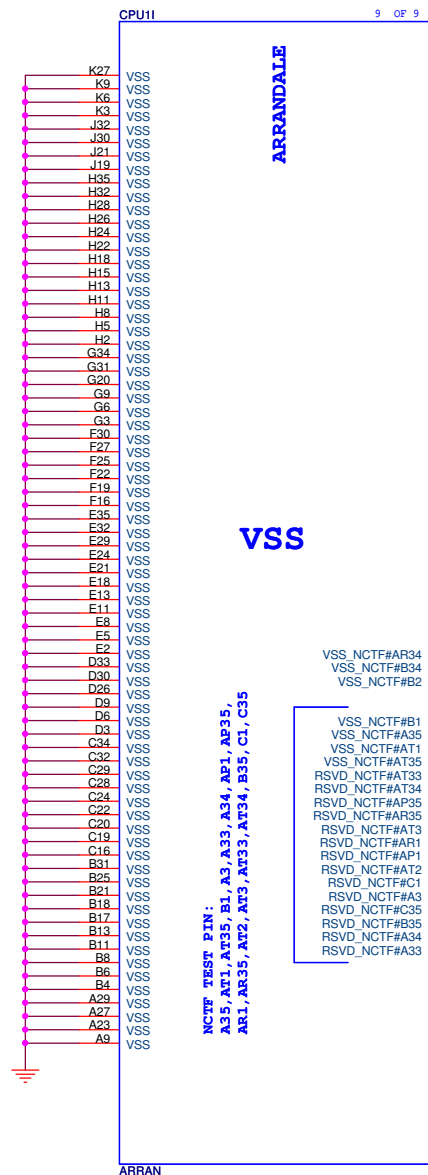
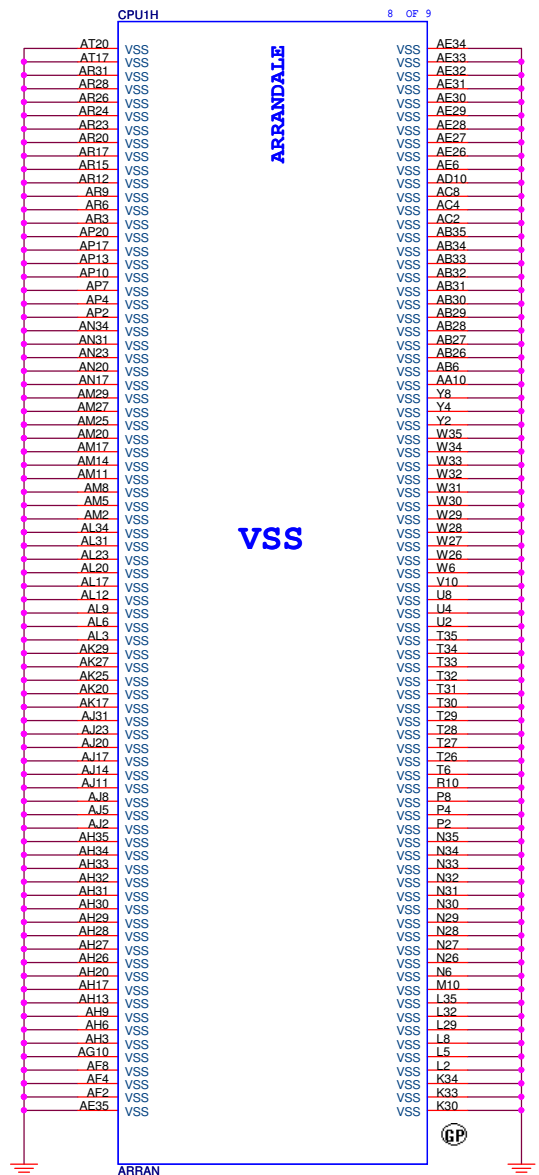
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Title CPU (VCC_CORE)

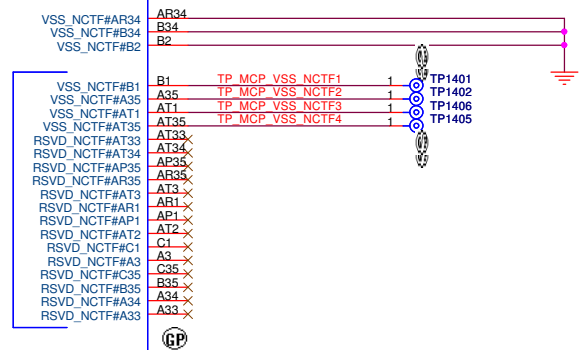
Size Document Number Rev A00

Date: Wednesday, April 13, 2011 Sheet 12 of 99





NCTF TEST PIN:
A35, AT1, AT35, B1, A3, A33, A34, AP1, AP35,
AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35



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Document Number

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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	

Reserved

Size
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Document Number

Enrico/Caruso 15 CP

Rev
A00

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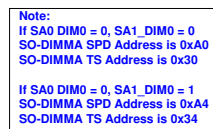
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Document Number

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Rev

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Layout Note:
Place these Caps near
SO-DIMMA.

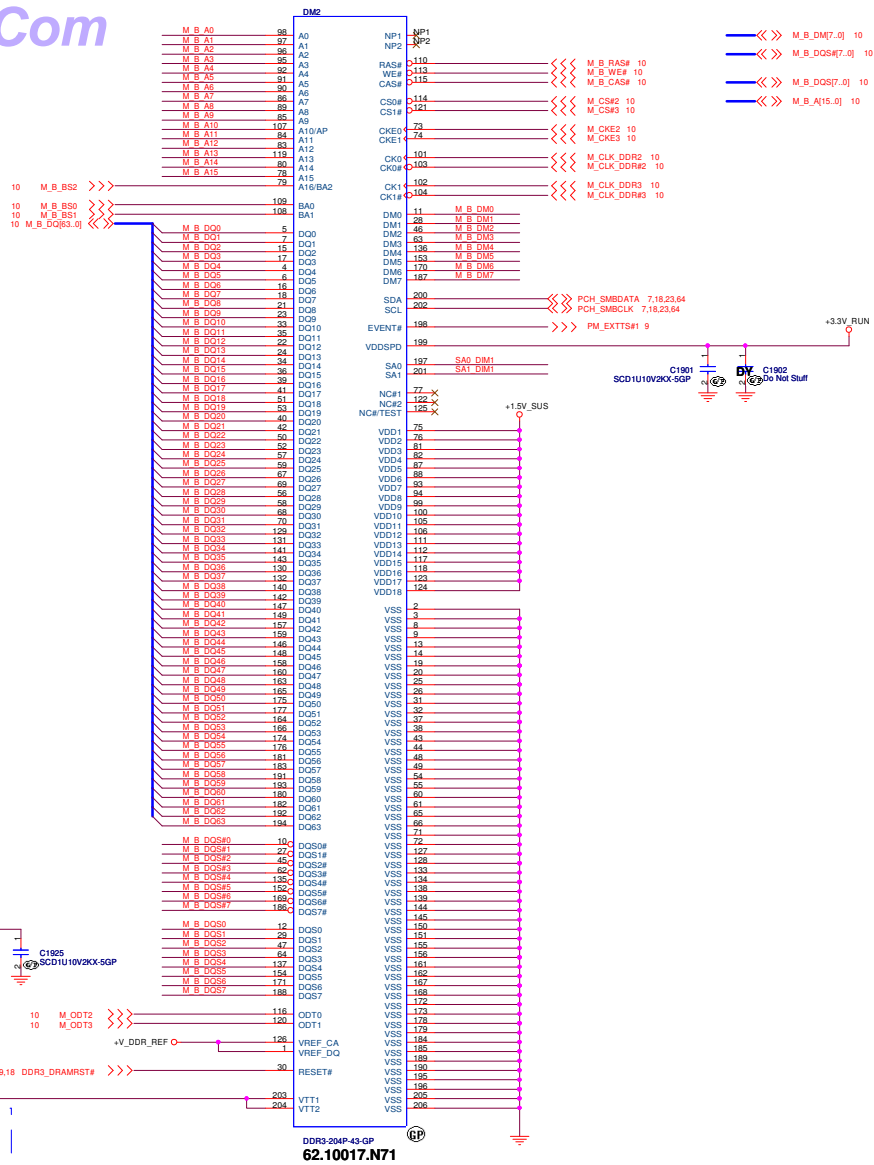
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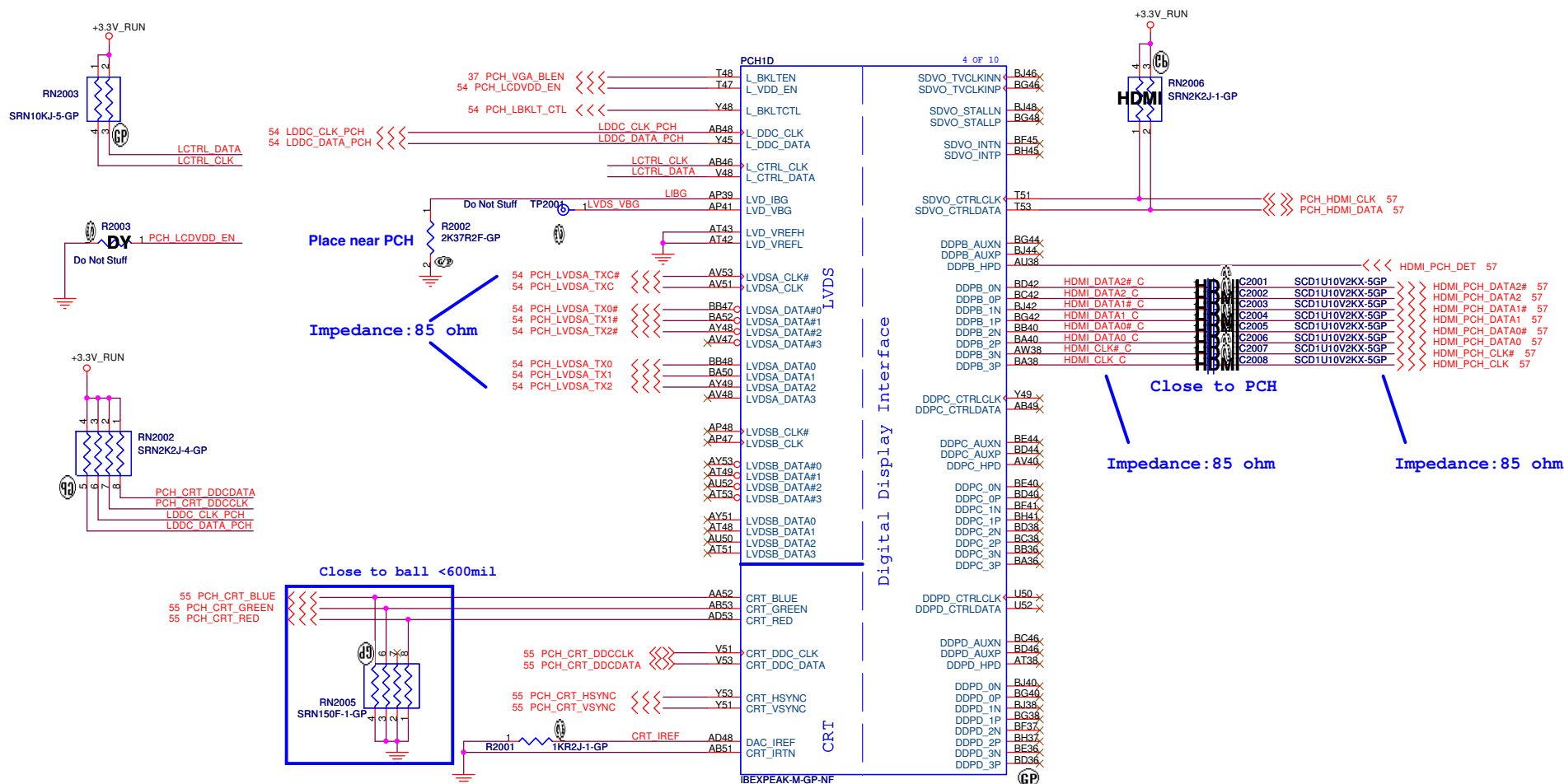
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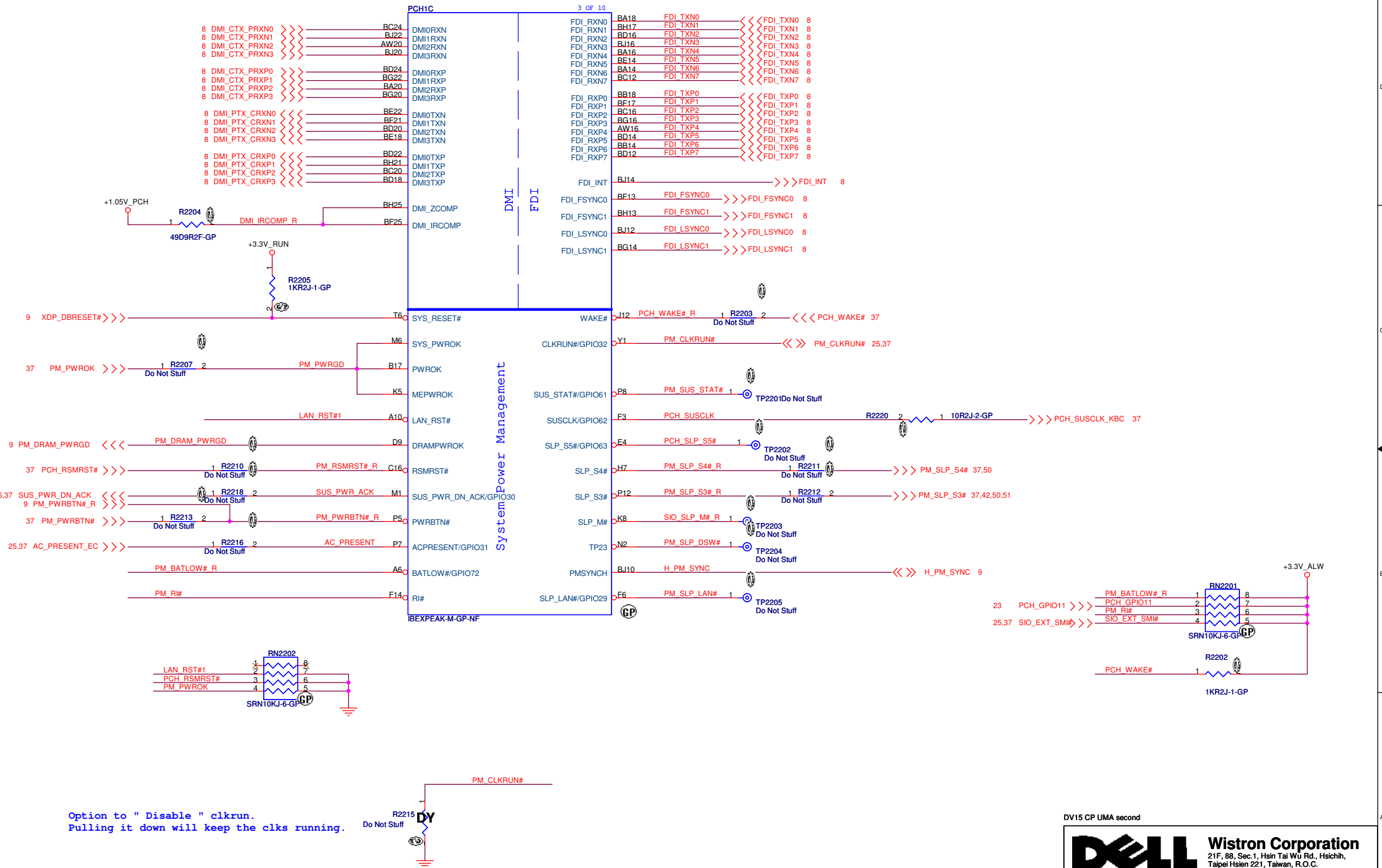


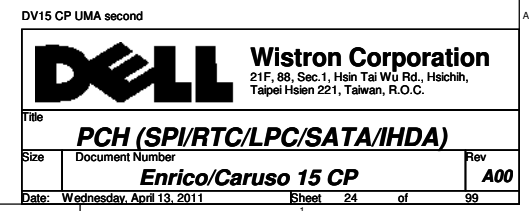
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Size	Document Number		Rev
	Enrico/Caruso 15 CP		A0
Date: Wednesday, April 13, 2011		Sheet 18 of	99

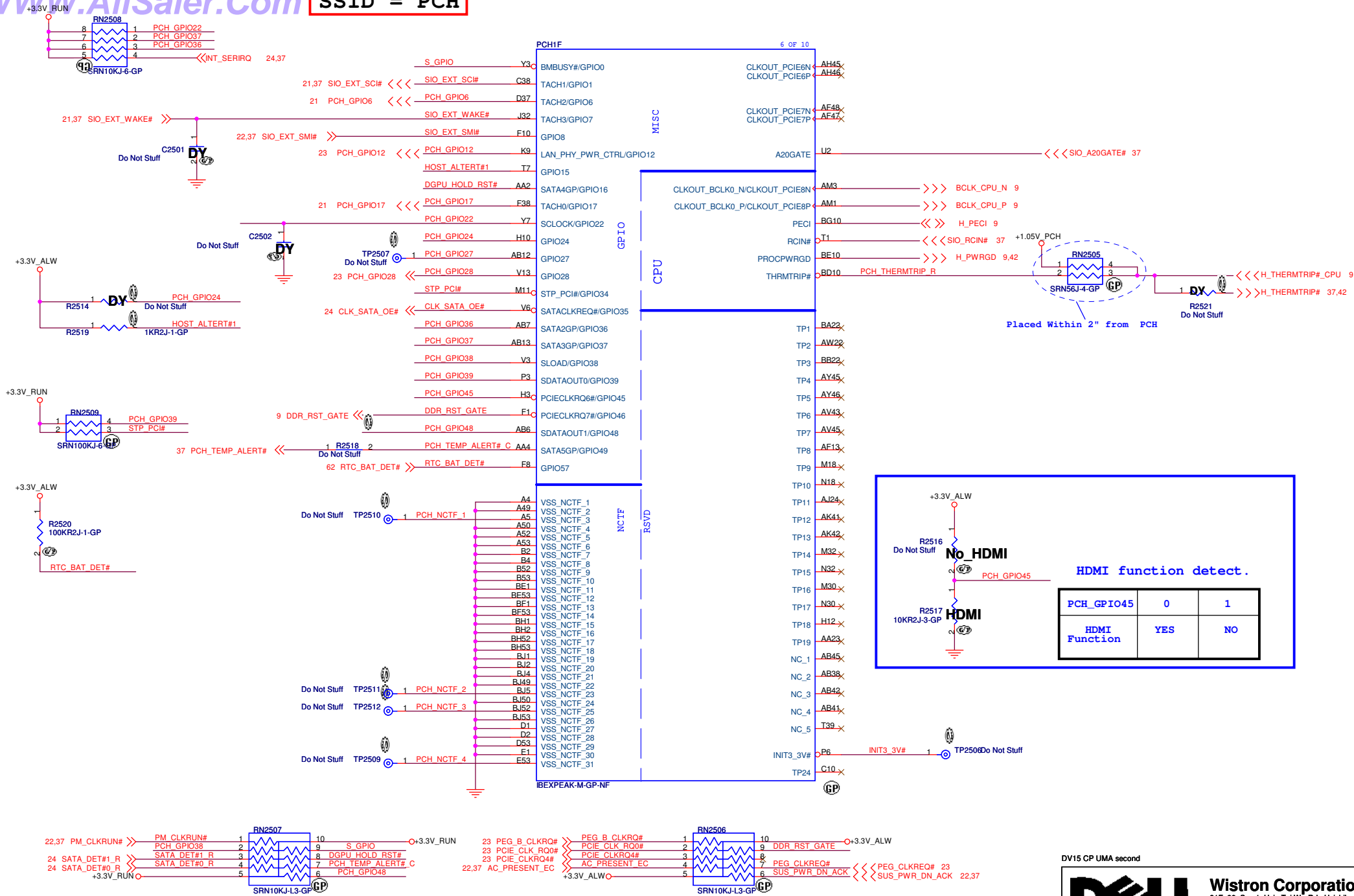








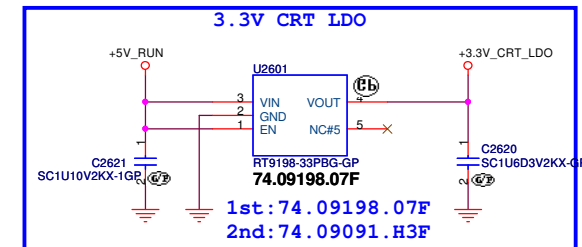


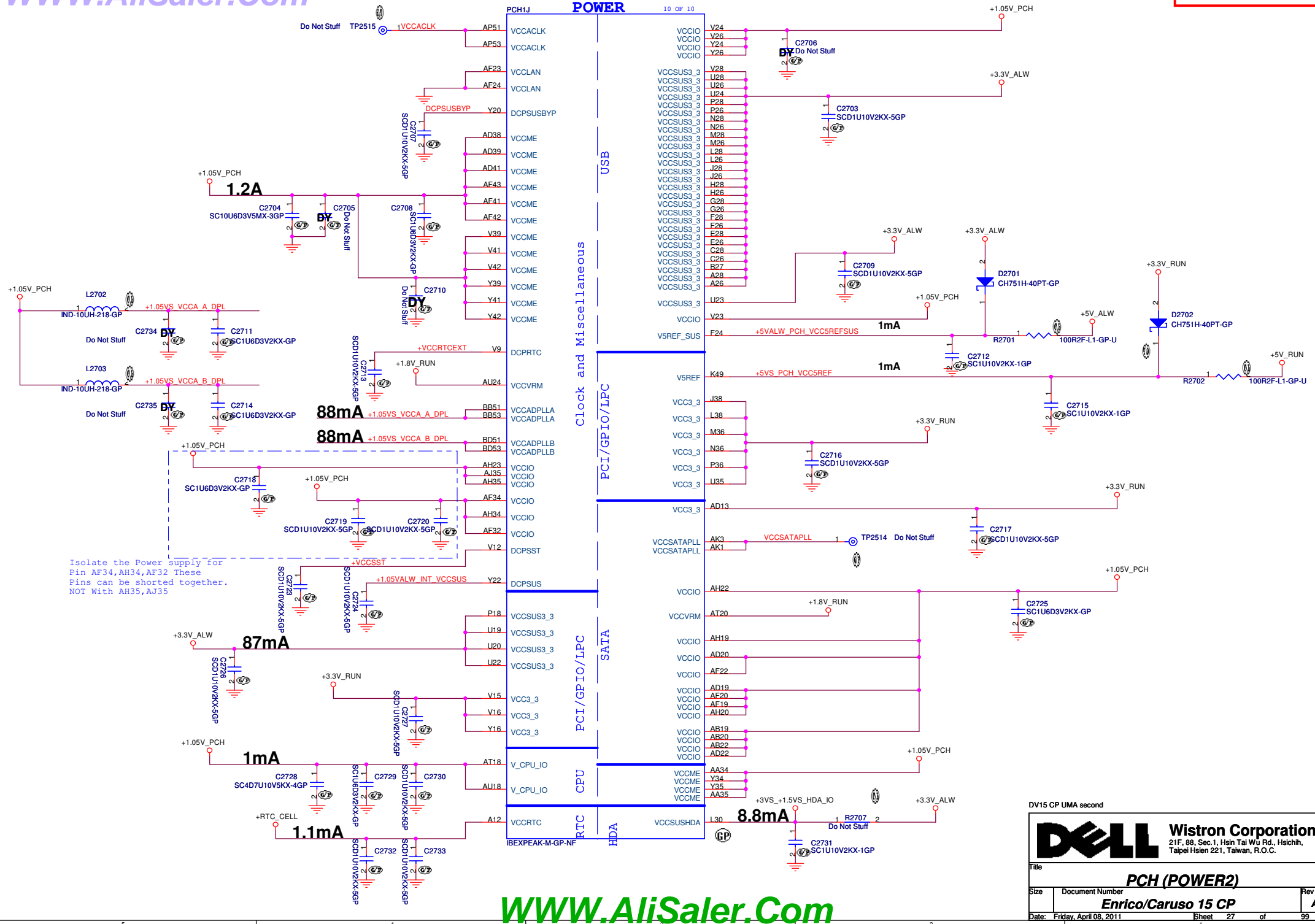


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PCH (VSS)				
Size	Document Number			Rev
	Enrico/Caruso 15 CP			A00
Date:	Friday, April 08, 2011		Sheet 28 of	99

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Document Number
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Rev
A00

Sheet 29 of 99



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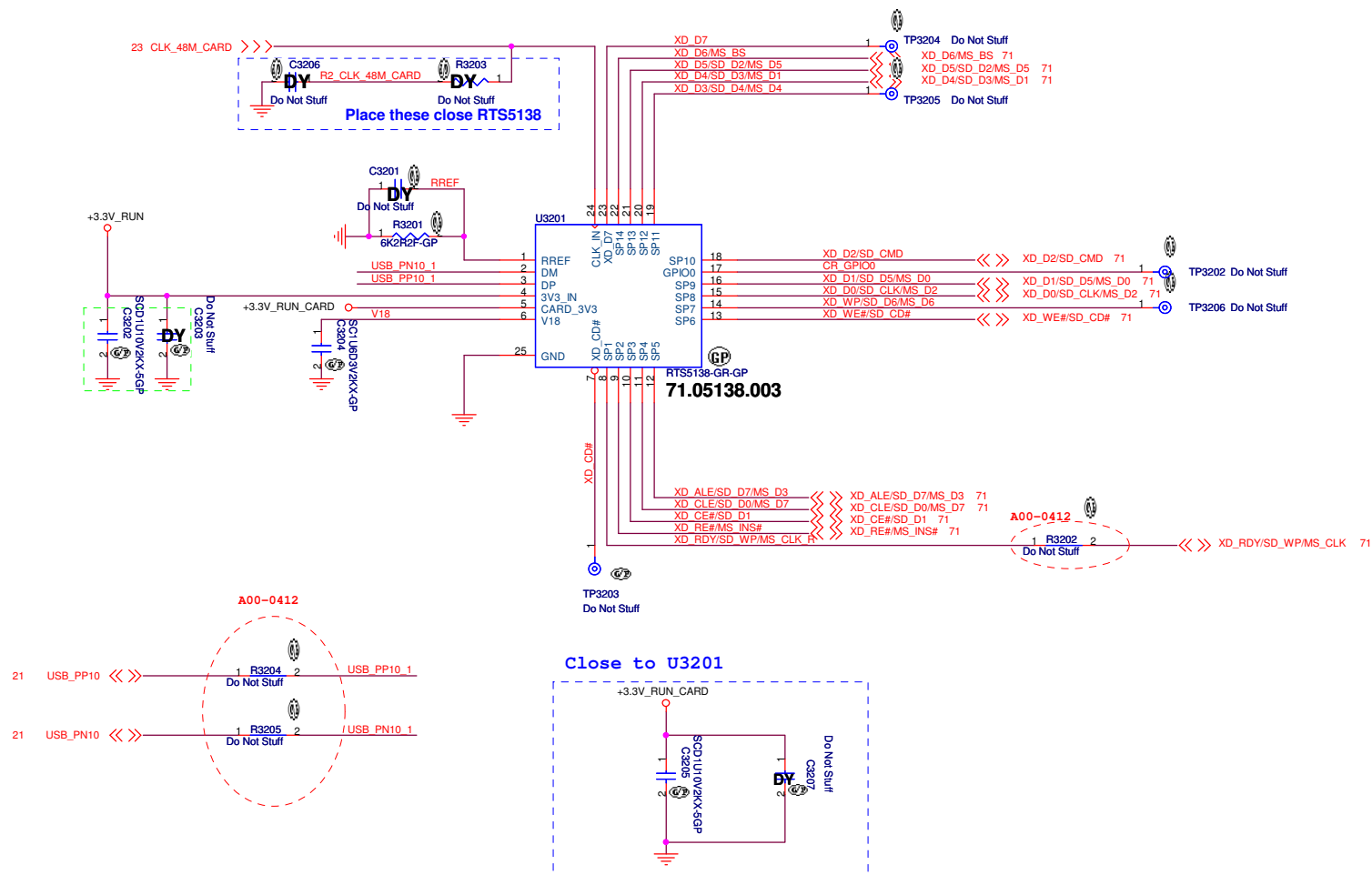
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Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date: Friday, April 08, 2011	Sheet 31 of 99	

SSID = SDIO



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		Title Card Reader-RTS5138	
Size Custom	Document Number Enrico/Caruso 15 CP	Rev A00	
Date: Wednesday, April 13, 2011		Sheet 32 of 99	

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Document Number
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Sheet 33 of 99

Rev
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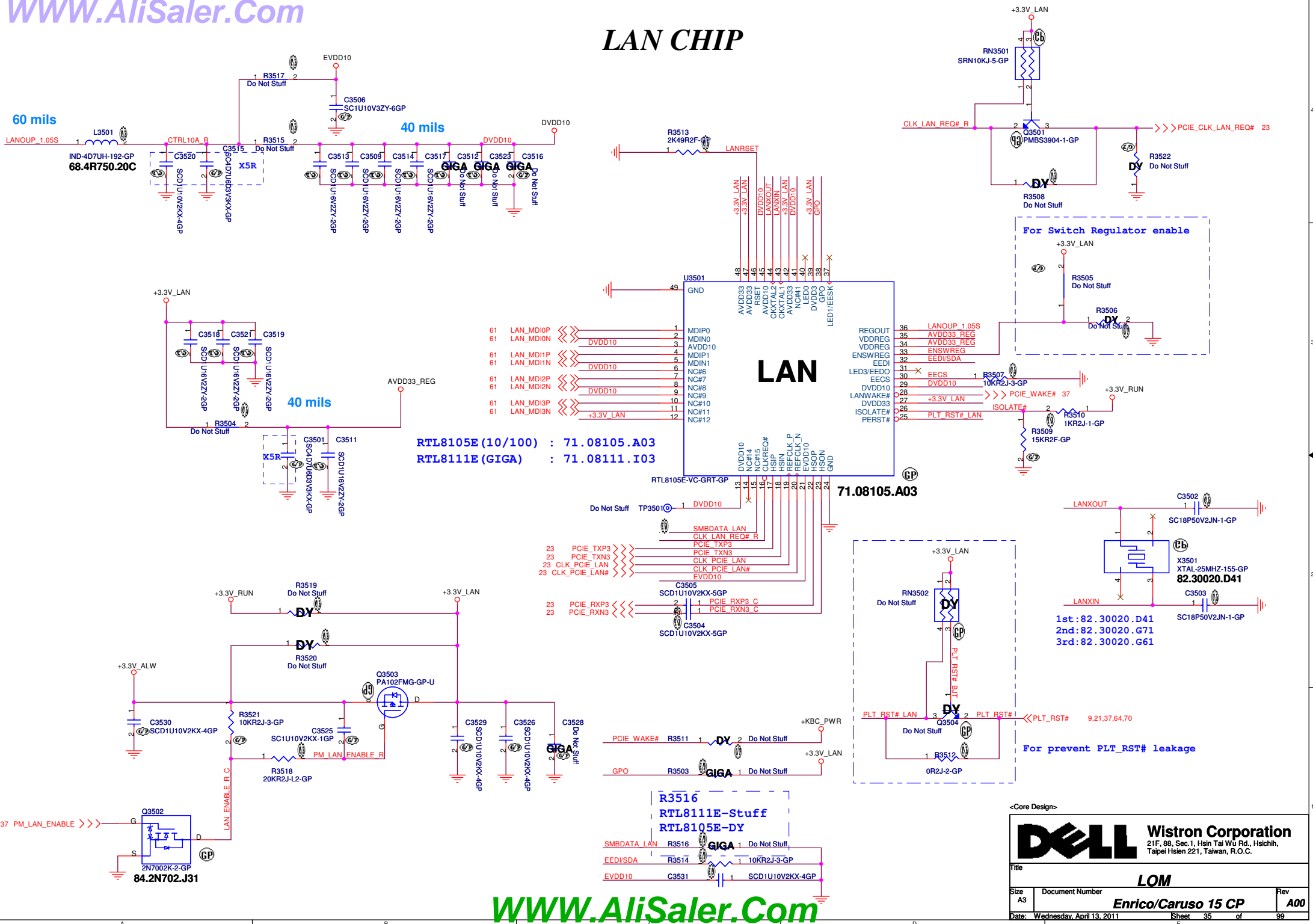
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Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Rev
A00

Sheet 34 of 99

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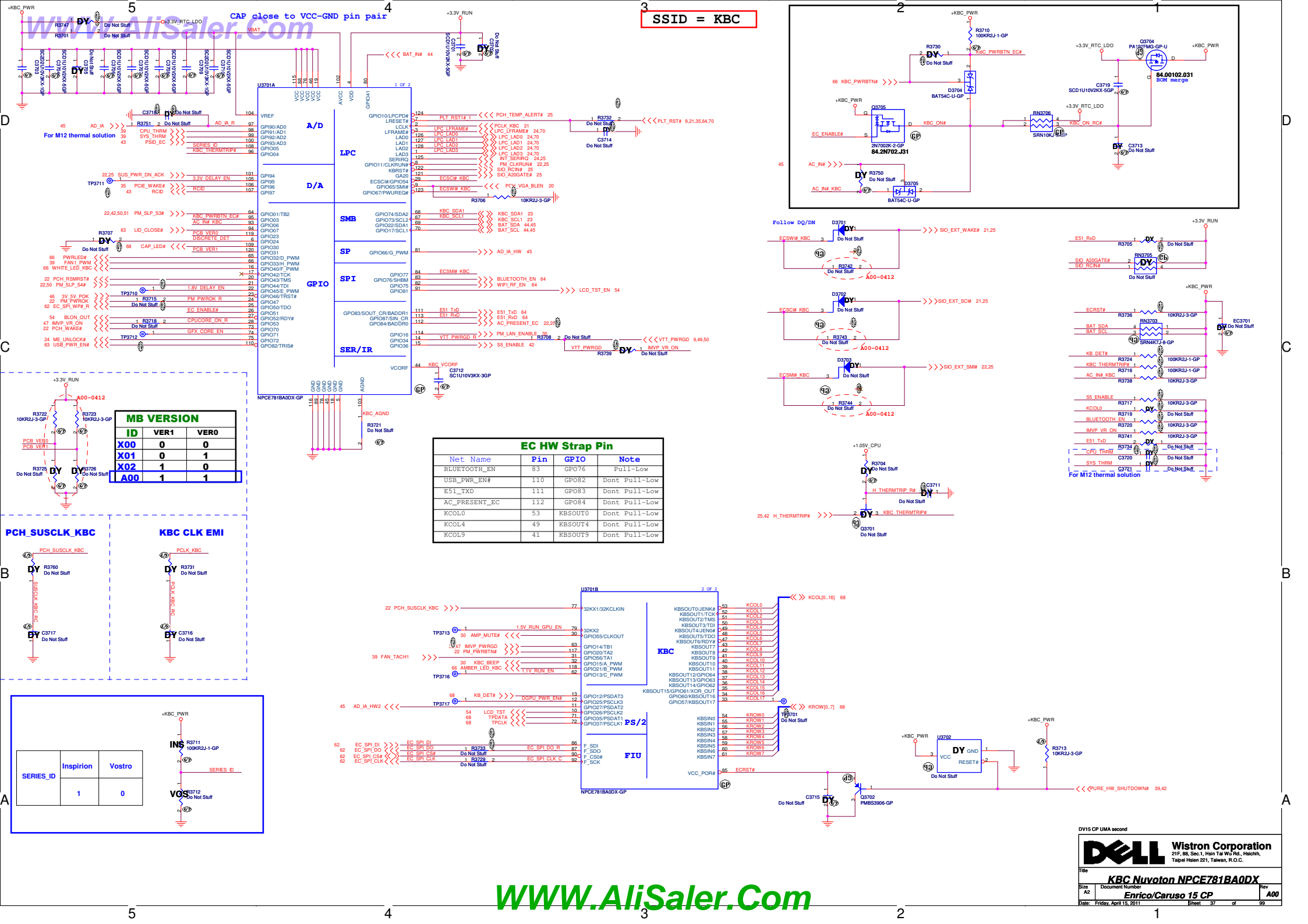
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Rev
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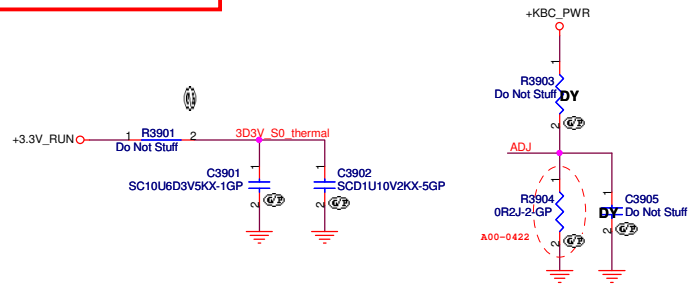
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Document Number
Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Sheet 38 of 99

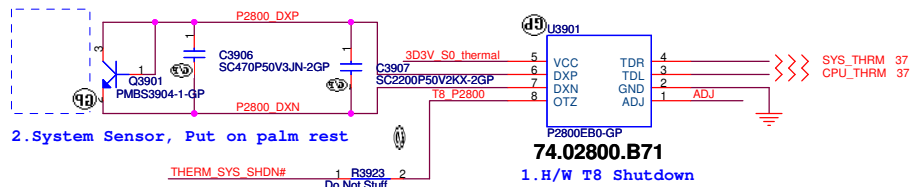
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Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

Thermal sensor P2800

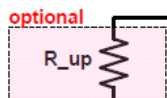
Remove R3908 and
put C3906 close to Q3901



2. System Sensor, Put on palm rest

THERM_SYS_SHDN#

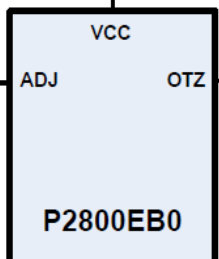
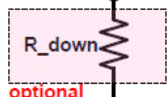
3.0V to 3.6V



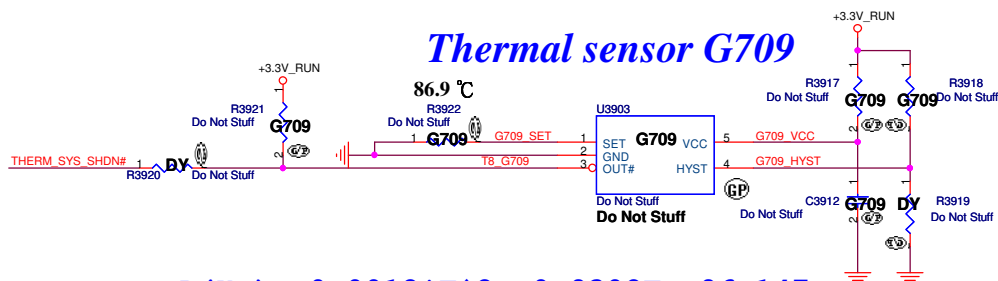
Option 1: OTZ=95°C → ADJ=3.3V

Option 2: OTZ=85°C → ADJ=Floating

Option 3: OTZ=90°C → ADJ=GND

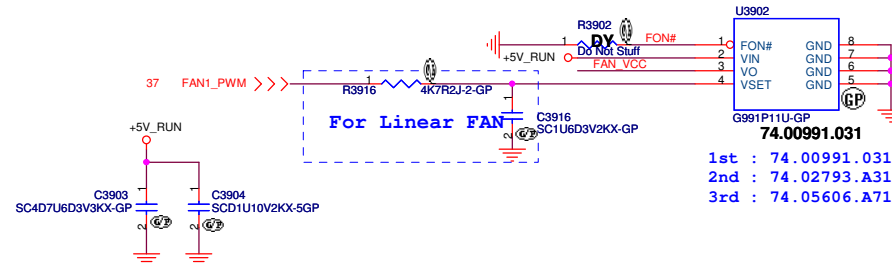


Thermal sensor G709



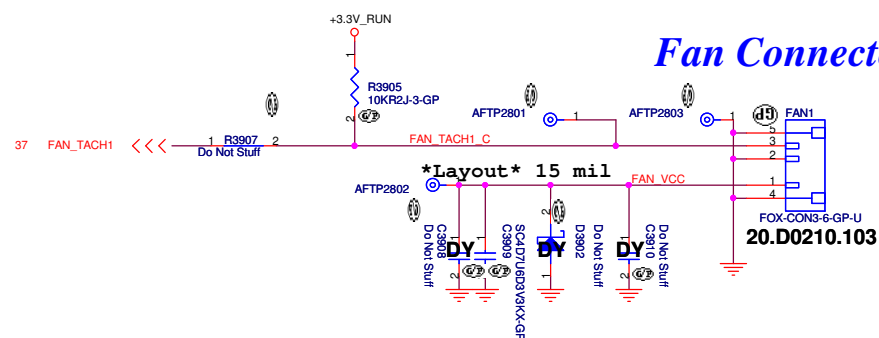
$$R(K\Omega) = 0.0012 * T^2 - 0.9308T + 96.147$$

Fan controller



1st : 74.00991.031
2nd : 74.02793.A31
3rd : 74.05606.A71

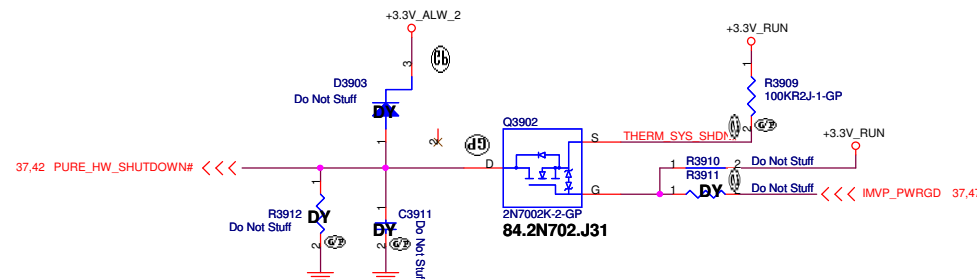
Fan Connector



37 FAN_TACH1 <<<

37.42 PURE_HW_SHUTDOWN# <<<

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number

Enrico/Caruso 15 CP

Date: Friday, April 08, 2011

Sheet 40 of 99

Rev

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Taipei Hsien 221, Taiwan, R.O.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

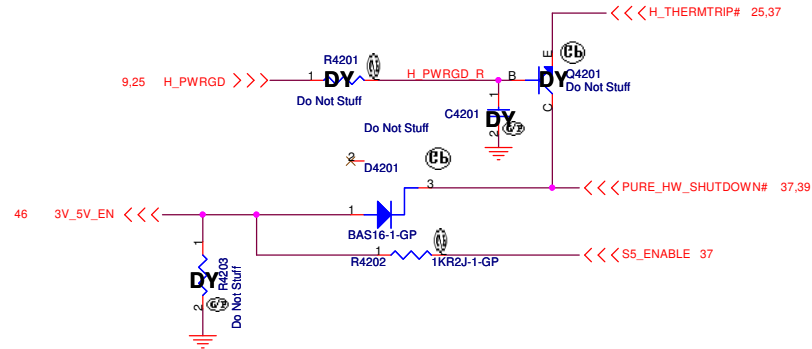
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Size
A3

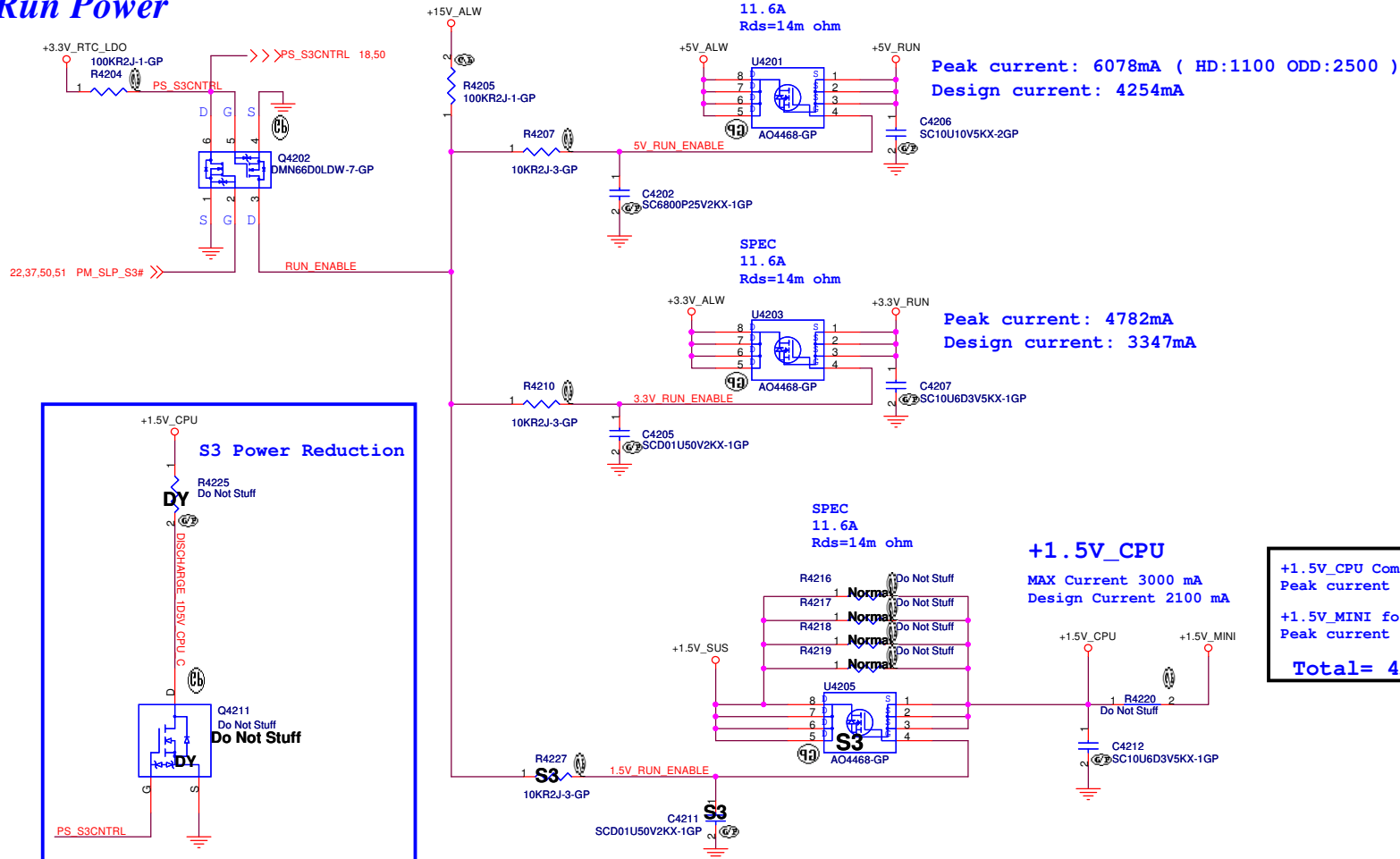
Document Number

Enrico/Caruso 15 CP

Rev
A00



Run Power

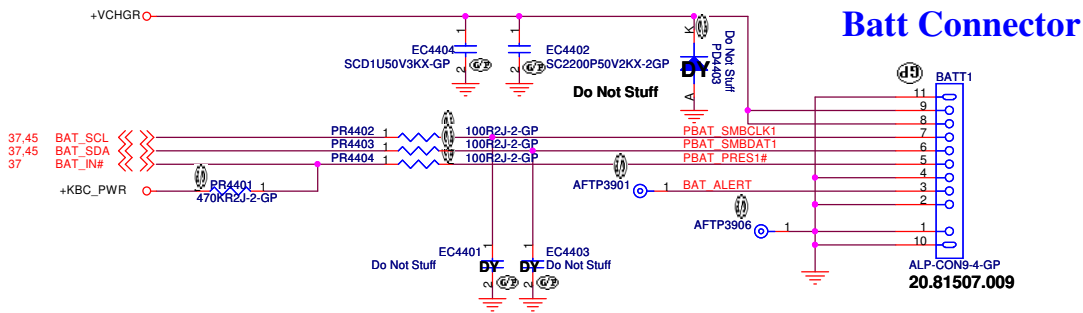


DV15 CP UMA second

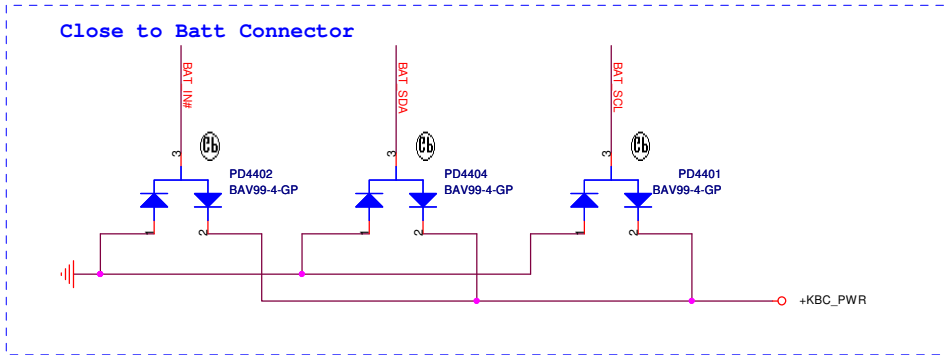


Power Plane Enable		
Size A3	Document Number	Rev
Enrico/Caruso 15 CP		A00
Date: Wednesday, April 13, 2011	Sheet 42	of 99

SSID = BATT CONN



For actual location, need to be swap all pin



<Core Design>



SSID = Charger

EE need pull high and net name

9.47 H_PROCHOT#

PR4505 Do Not Stuff

PR4504 10KR2J-3-GP

PR4503 100KR2J-1-GP

PR4502 100KR2F-2-GP

PR4501 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

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PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

PR4500 100KR2F-2-GP

ROSA

Adapter Type	PR4522
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

EE need check pull high

Charger Current=1.4~3.6A

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<Core Design>

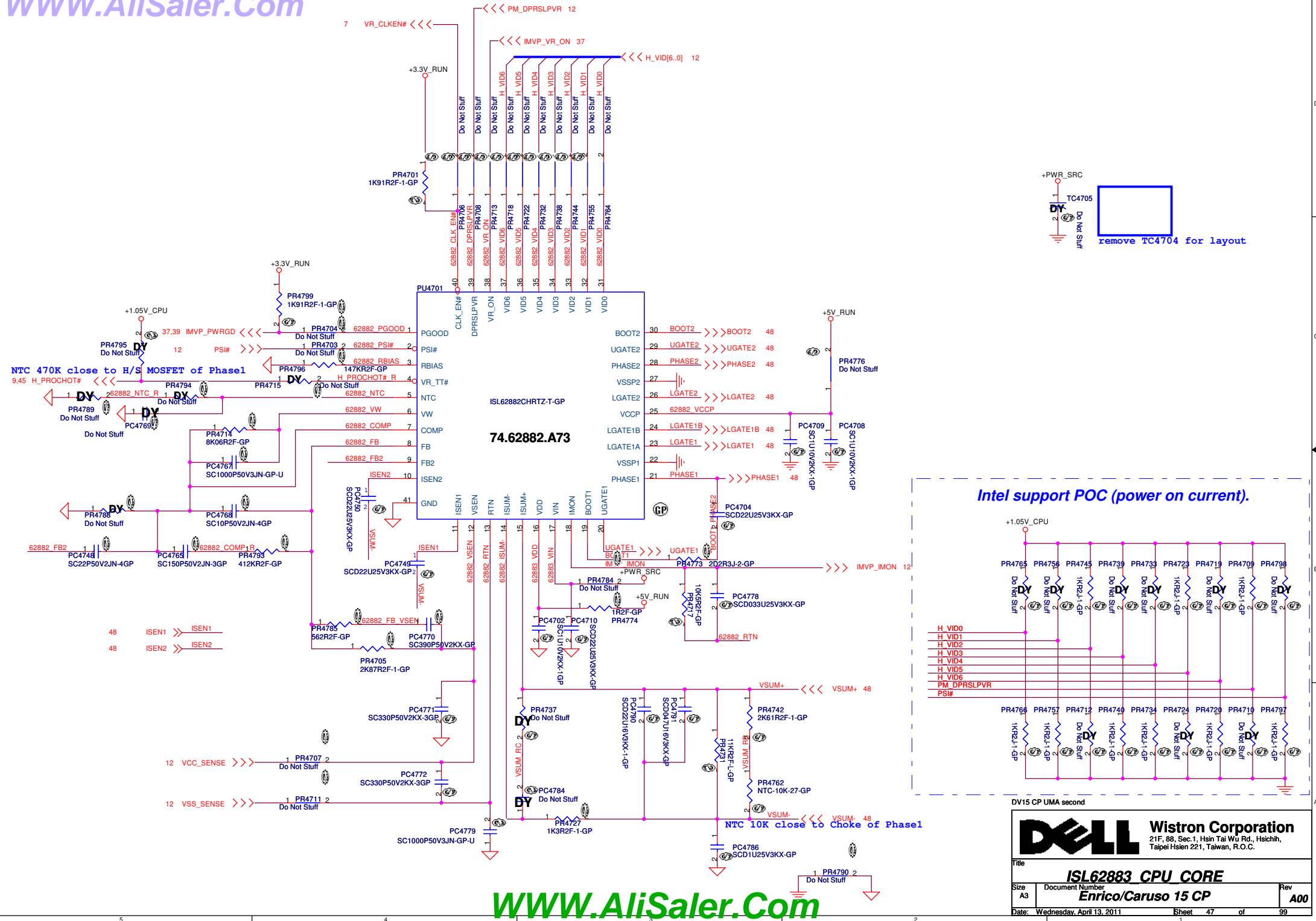
DELL Wistron Corporation
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Taipai Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24707**

Size	Document Number	Rev
Custom	Enrico/Caruso 15 CP	A00

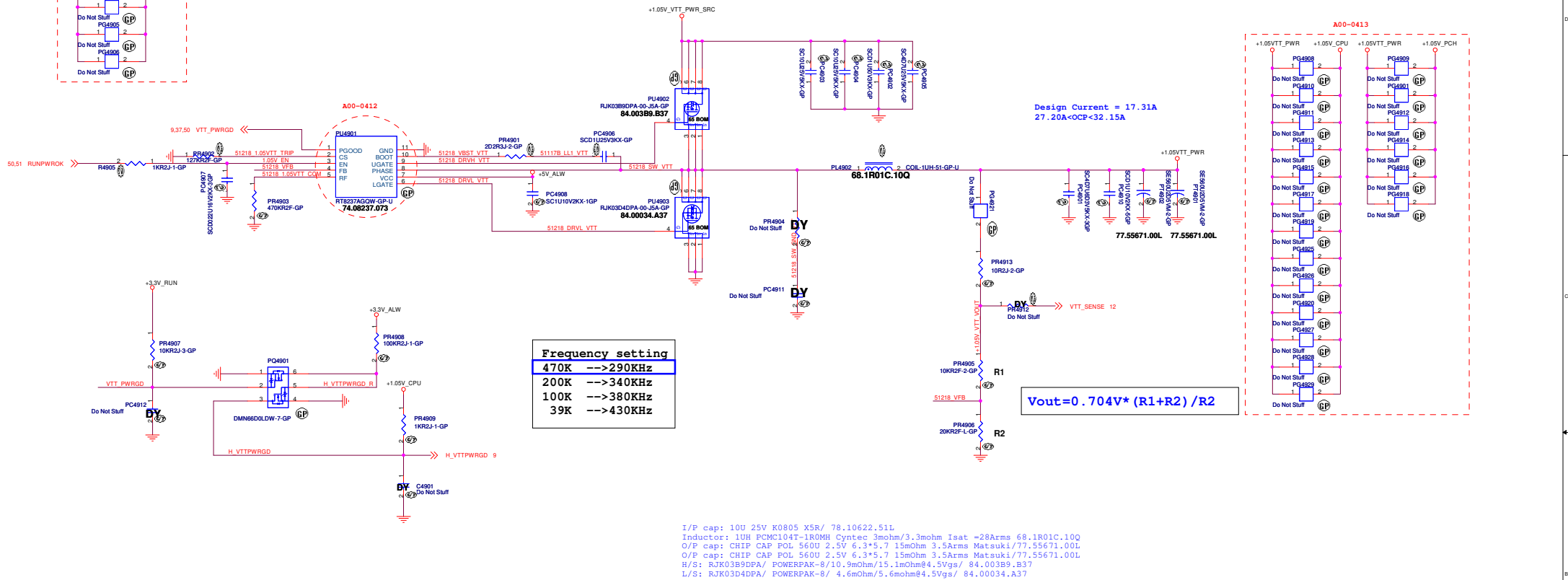
Date: Friday, April 15, 2011 Sheet 45 of 99



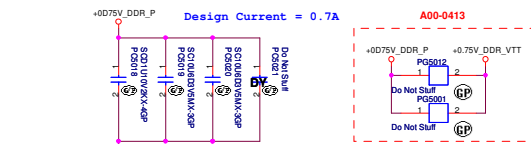


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RT8237A for +1.05V_VTT



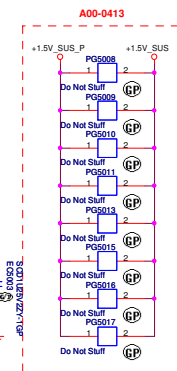
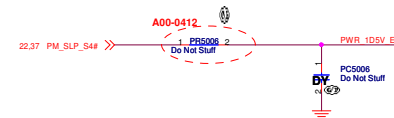
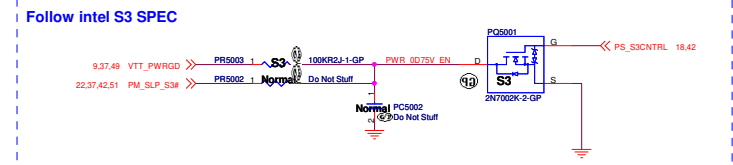
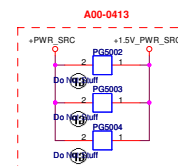
```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



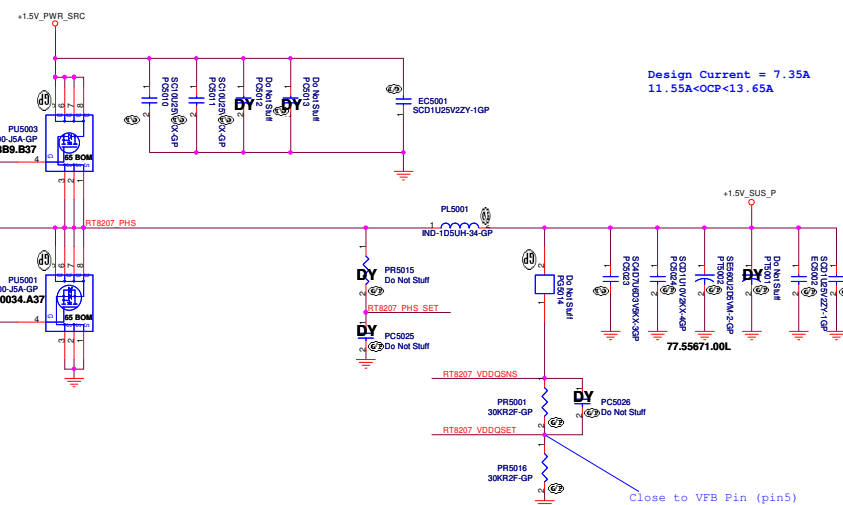
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 100 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5U PCCM104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: CHIP CAP POL 560U 2V 5.6 3.5*7 15mOhm 3.5Arms Matsuki/77.55671.00L
H/S: RJK0389DPA/ POWERPAK-8/10..9mOhm/15.1mOhm@4.5Vgs/ 84.00389..B37
L/S: RJK0342DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37



Design Current = 7.35A
11.55A<OCP<13.65A



Close to VFB Pin (pin5)

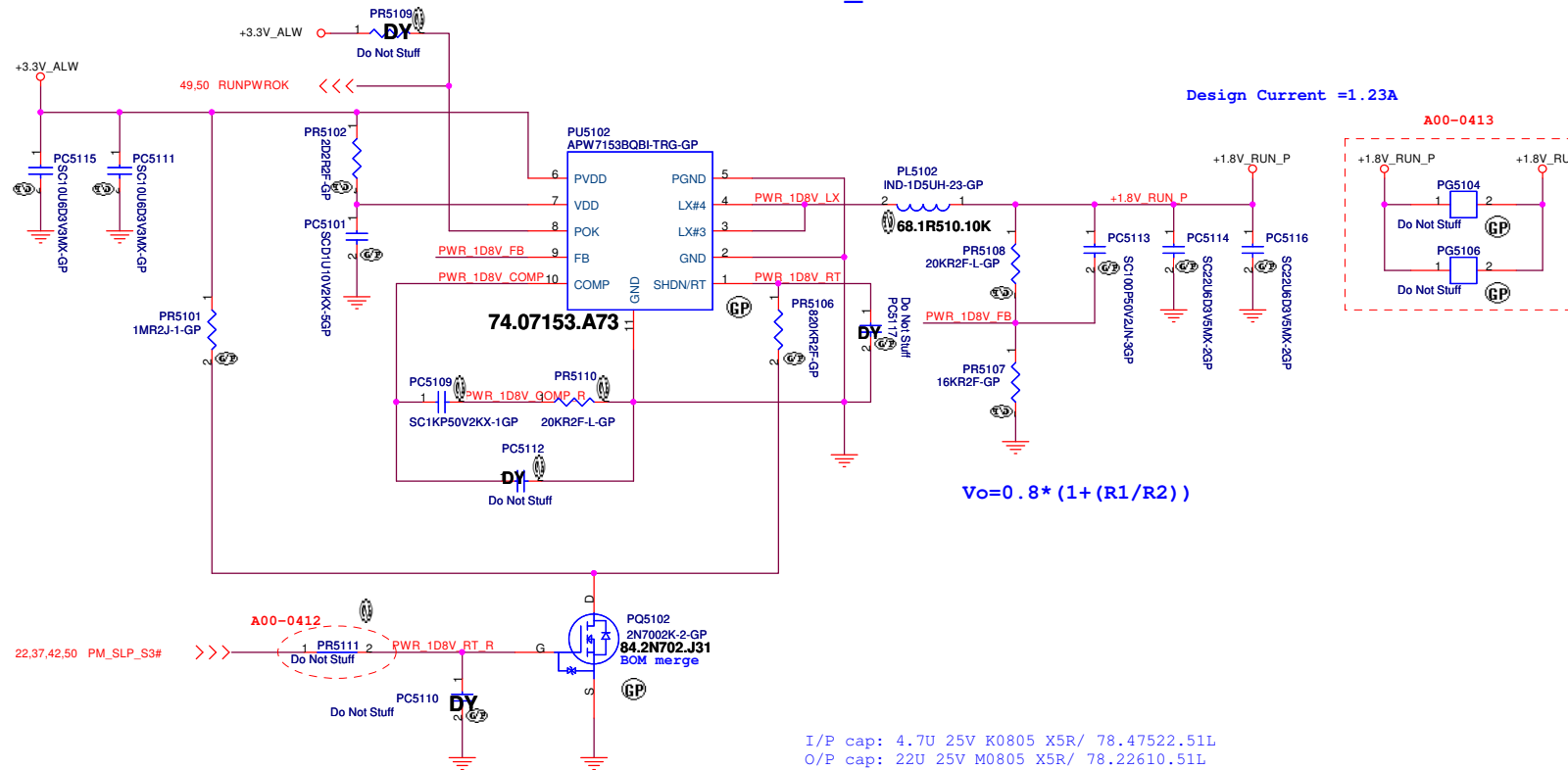
&ltCore Design>



Title			
RT8207 +1.5V SUS			
Size A2	Document Number		Rev
	Enrico/Caruso 15 CP		A00
Date:	Wednesday, April 13, 2011		Sheet 50 of 99

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APW7153B for 1D8V_RUN



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: CHIP CHOKE 1.5U PCMC063T-1R5MN Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K



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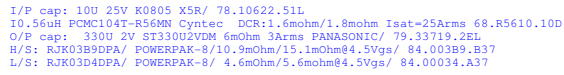
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Size
A3

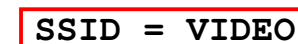
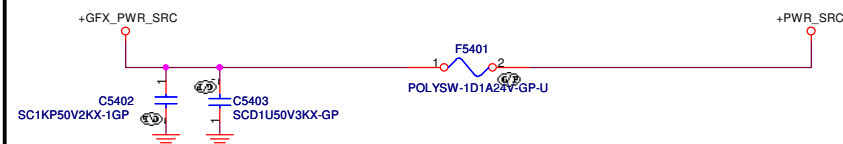
Document Number

Enrico/Caruso 15 CP

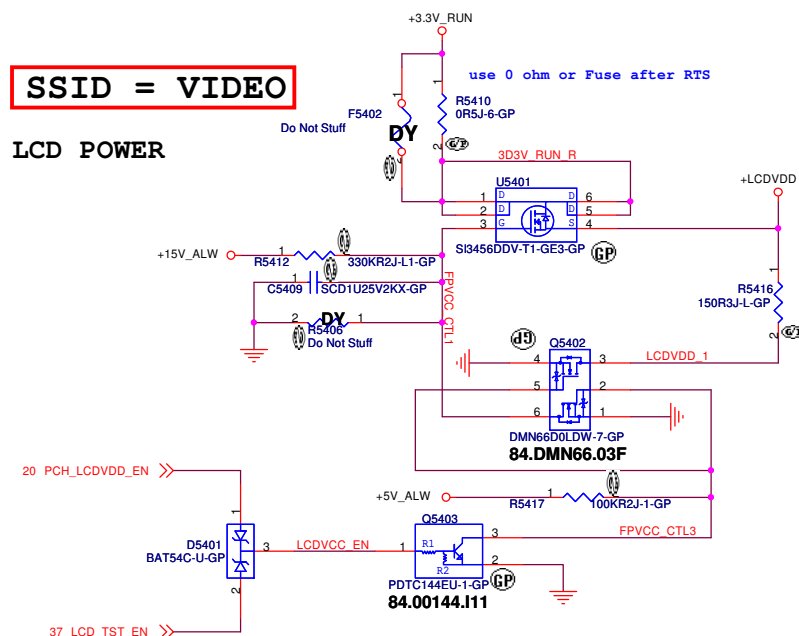
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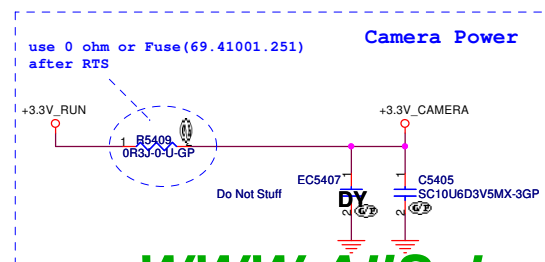
INVERTER POWER



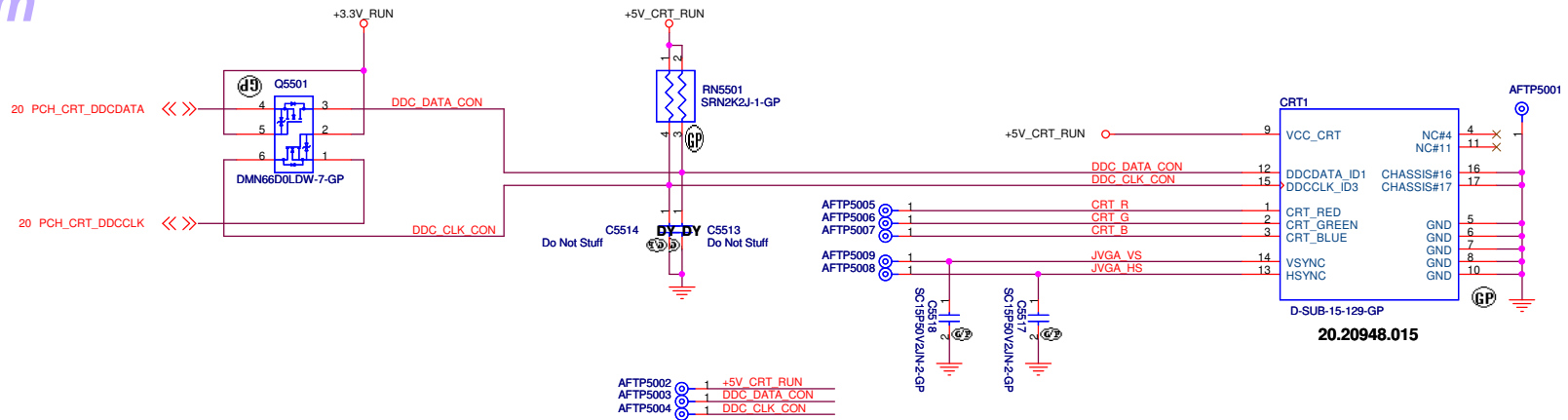
SSID = VIDEO use 0 ohm or Fuse after RTS



DV15 CP UMA second

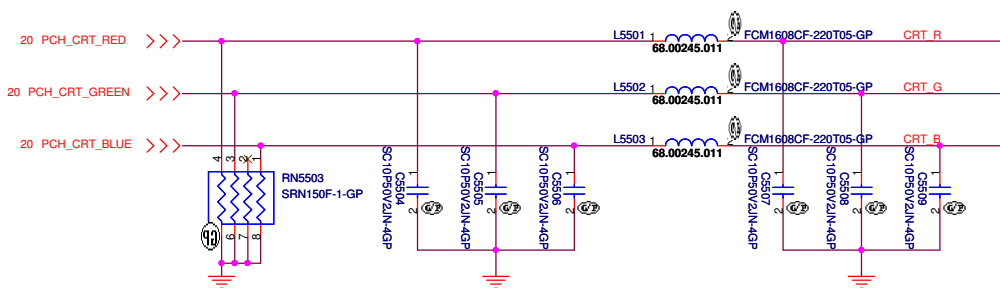


Title			
LCD/Inverter Connector			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 CP	A00	
Date:	Wednesday, April 13, 2011	Sheet	54 of 99

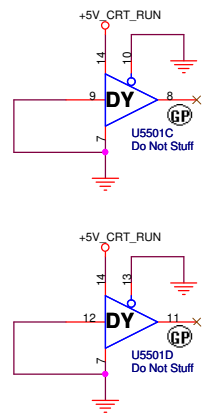
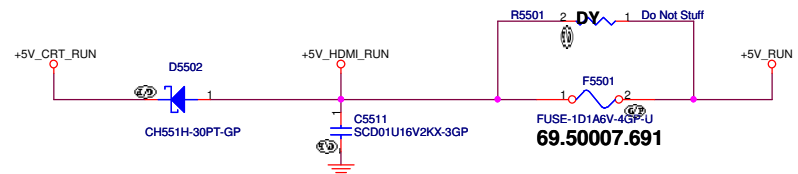
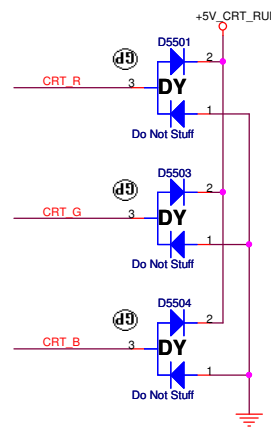
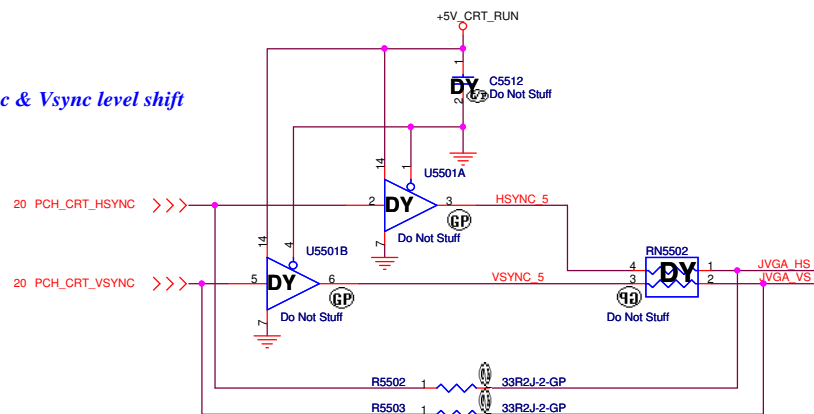


Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



DV15 CP UMA second

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Title CRT Connector		
Size	Document Number	Rev
	Enrico/Caruso 15 CP	A00
Date:	Wednesday, April 13, 2011	Sheet 55 of 99

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Title	Author	Date	Page
Title	Author	Date	Page
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Size	A3
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Document Number

Enrico/Caruso 15 CP

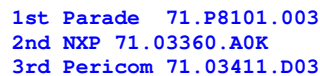
Rev

A00

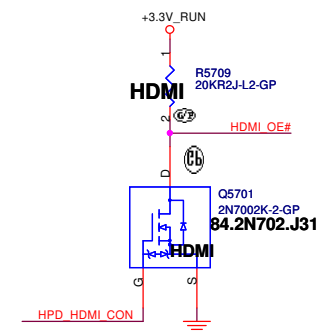


		PS8101	PTN3360E	PI3VDP411LS
PIN3	R5703	Stuff 4.7K_5%	DY	DY
PIN4	R5704	DY	DY	DY
	R5706	DY	DY	Stuff 200K_5%
PIN6	R5705	Stuff 499_1%	Stuff 10K_1%	DY
PIN10		NC	NC	NC

HDMI CONN

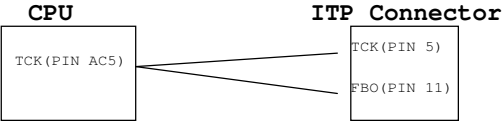


A00-0412



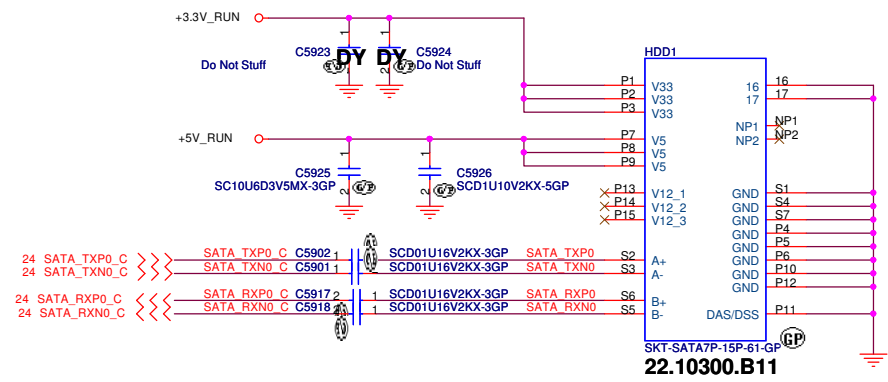
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



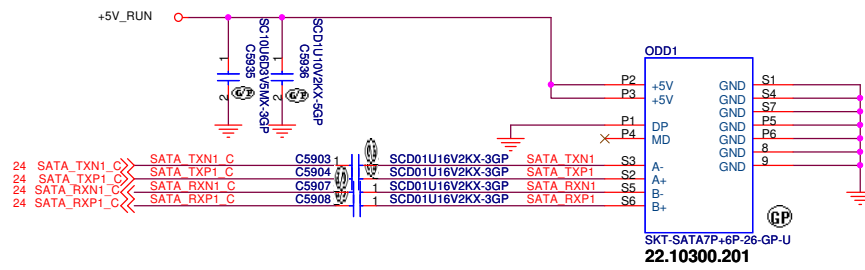
REMOVE FAN CONNECTOR FOR HR THERMAL SOLUTION 7/12

SATA HDD Connector



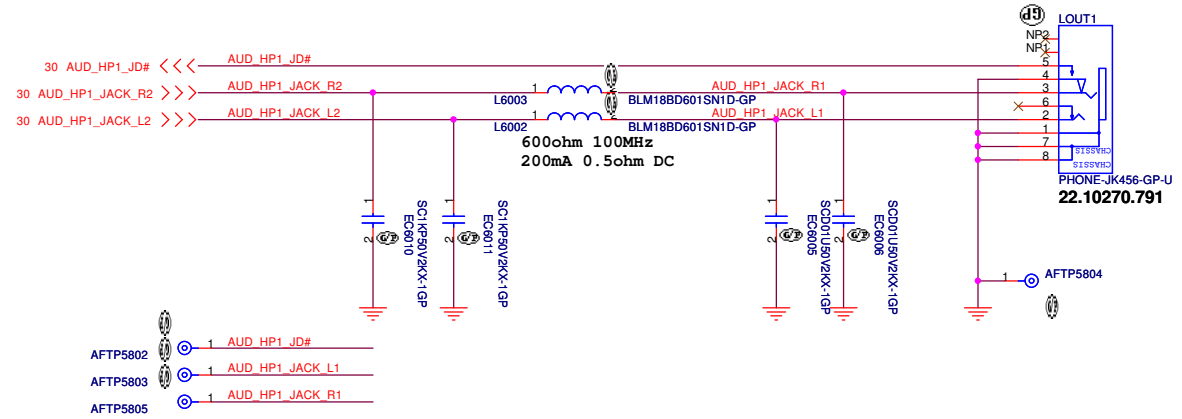
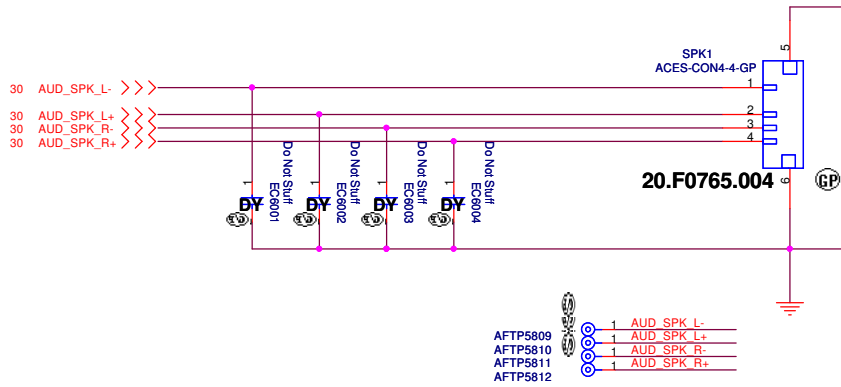
SATA ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



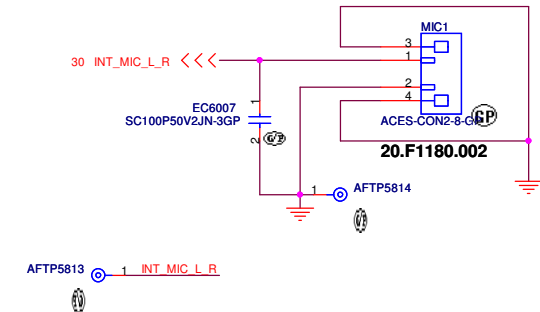
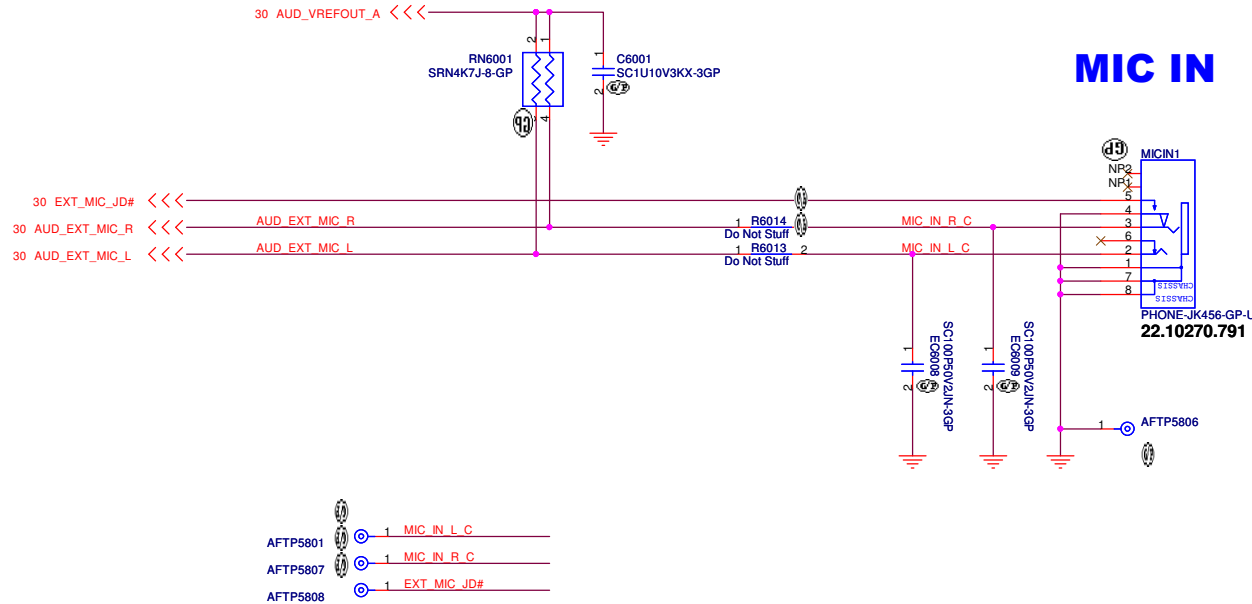
Speaker Connector

LINE1 OUT



MIC IN

Internal Microphone

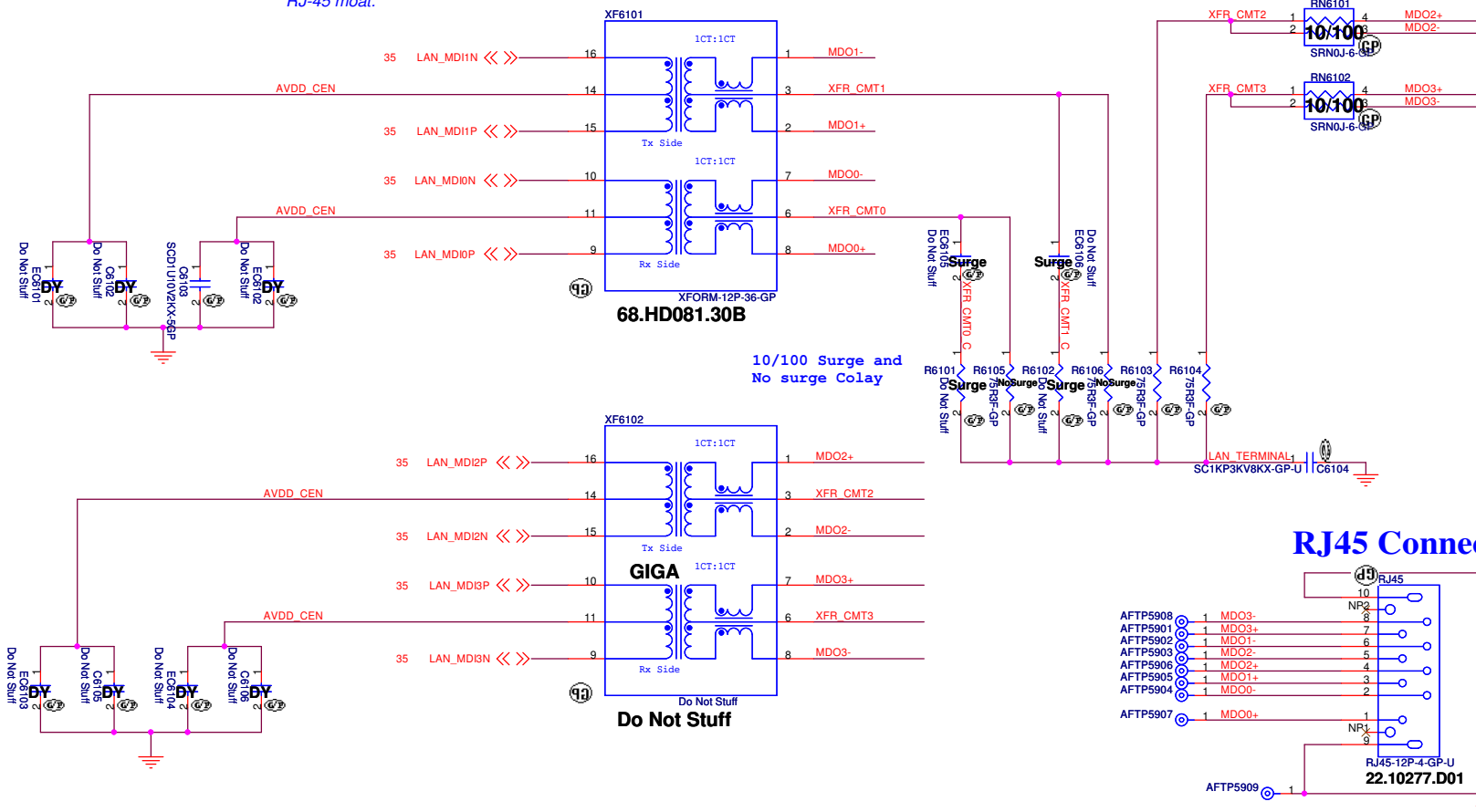


DV15 CP UMA second

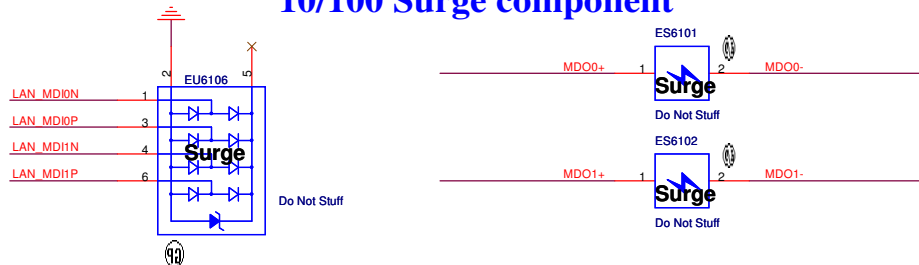
2009-10-1 Change MDI1+ (XF601.16) to MDI1+ (XF601.15)
 Change MDI1- (XF601.15) to MDI1- (XF601.16)
 Change MDI0+ (XF601.10) to MDI0+ (XF601.9)
 Change MDI0- (XF601.9) to MDI0- (XF601.10)
 Change RJ45-3 (XF601.1) to RJ45-3 (XF601.2)
 Change RJ45-6 (XF601.2) to RJ45-6 (XF601.1)
 Change RJ45-1 (XF601.7) to RJ45-1 (XF601.8)
 Change RJ45-2 (XF601.8) to RJ45-2 (XF601.7)

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

10/100M Lan Transformer



10/100 Surge component



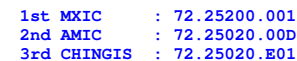
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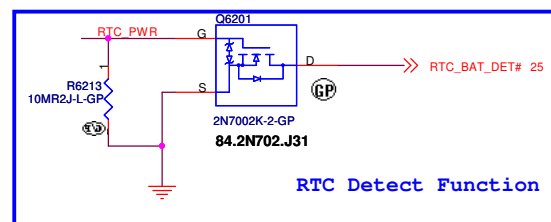
LAN Conn			
Size A3	Document Number	Rev A00	
Enrico/Caruso 15 CP			
Date: Wednesday, April 13, 2011	Sheet 61	of 99	

SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



DV15 CP UMA second

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Title

Flash/RTC

Size
A3

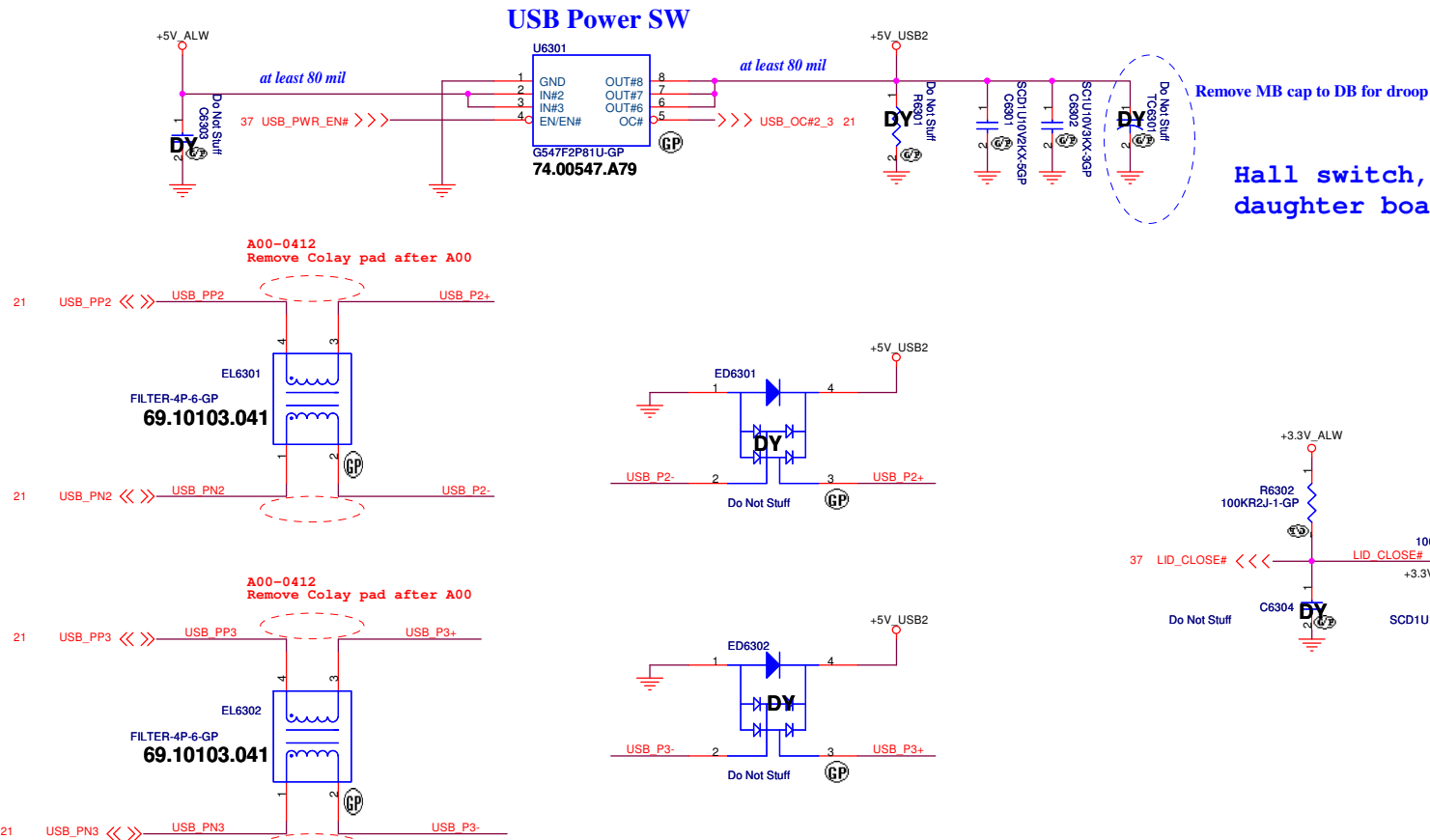
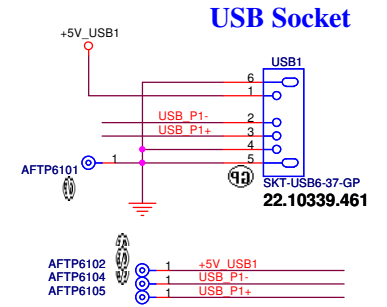
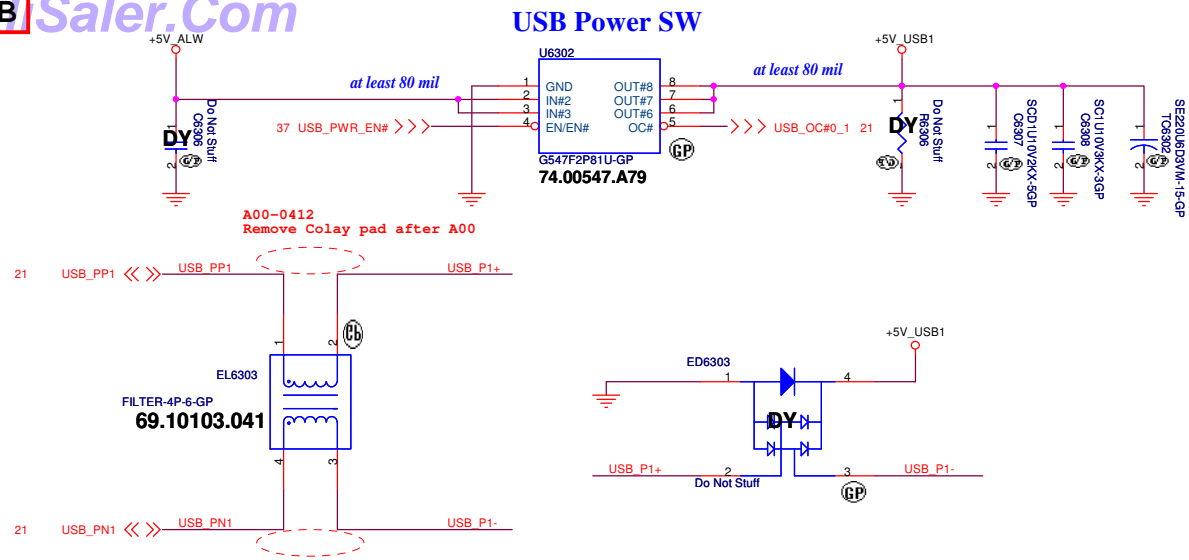
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Enrico/Caruso 15 CP

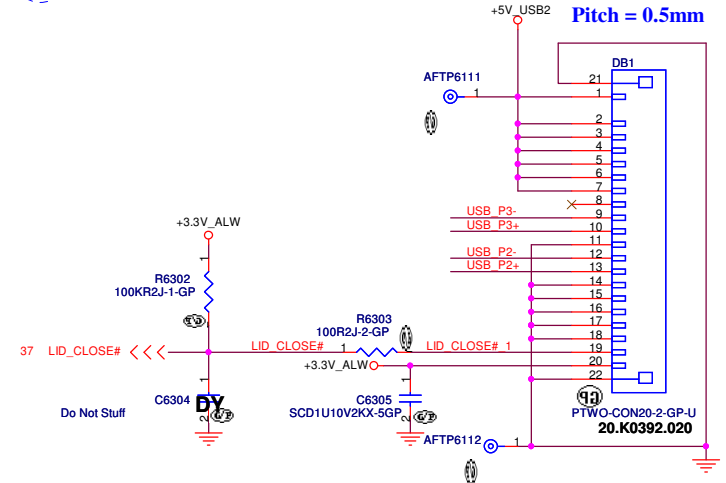
Rev	A00
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Date: Wednesday, April 13, 2011

Sheet 62 of 99

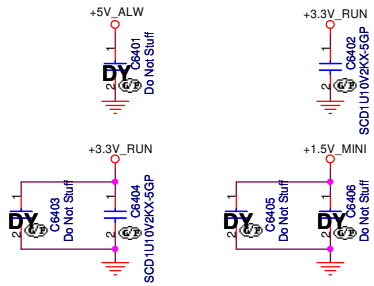
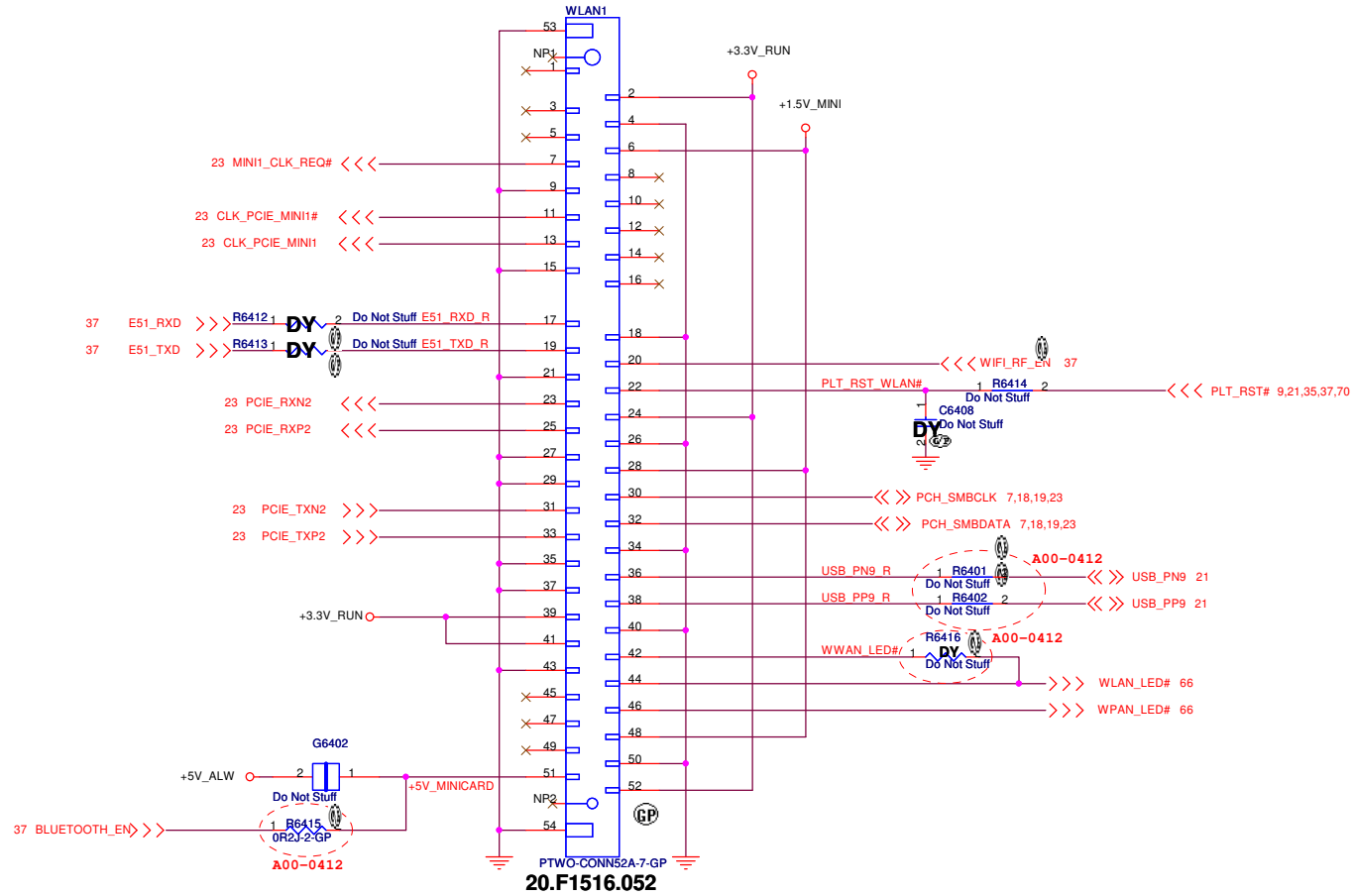


Hall switch, USB2 and USB3 go to daughter board through FFC



DV15 CP UMA second

Mini Card Connector(802.11a/b/g)



DV15 CP UMA second

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MINICARD			
Size A3	Document Number	Rev	
	Enrico/Caruso 15 CP	A00	
Date: Wednesday, April 13, 2011	Sheet 64	of	99

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No.	Title	Author	Date	Place
1	The Great Gatsby	F. Scott Fitzgerald	1925	New York
2	The Catcher in the Rye	J. D. Salinger	1951	New York
3	The Sound and the Fury	William Faulkner	1929	New York
4	The Waste Land	T. S. Eliot	1922	New York
5	The Sun Also Rises	Ernest Hemingway	1926	New York
6	The Grapes of Wrath	John Steinbeck	1939	New York
7	The Old Man and the Sea	Ernest Hemingway	1952	New York
8	The Great American Novel	Various Authors	1950s	New York
9	The American Dream	Various Authors	1950s	New York
10	The American Dream	Various Authors	1950s	New York

Reserved

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A3

Document Number

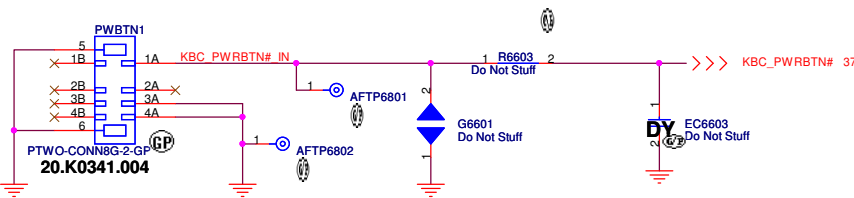
Enrico/Caruso 15 CP

Rev

A00

SSID = User.Interface

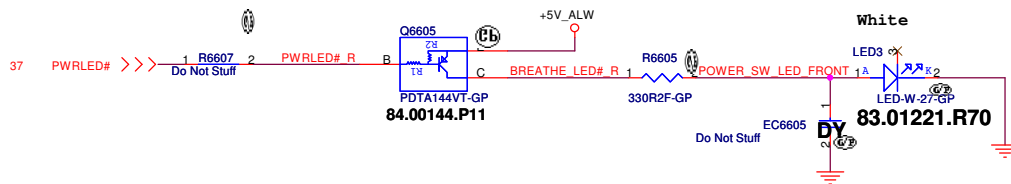
Power BTN Connector



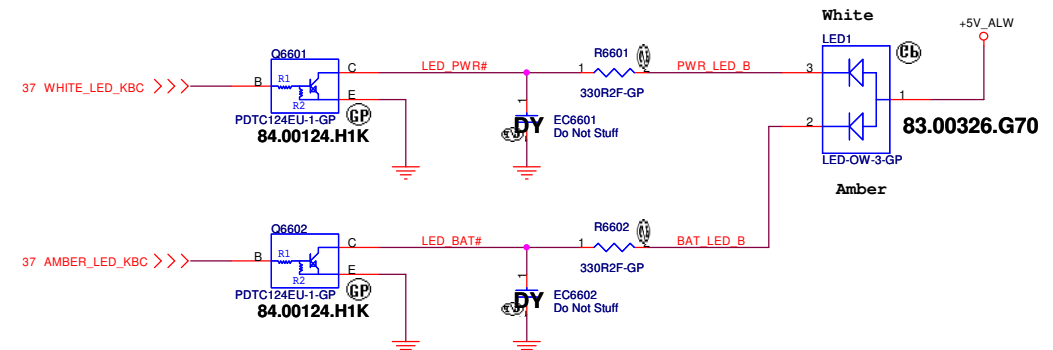
LED Location from left to right
(MB, Top View)

LED3 PWR LED2 HDD LED1 Battery LED4 WLAN

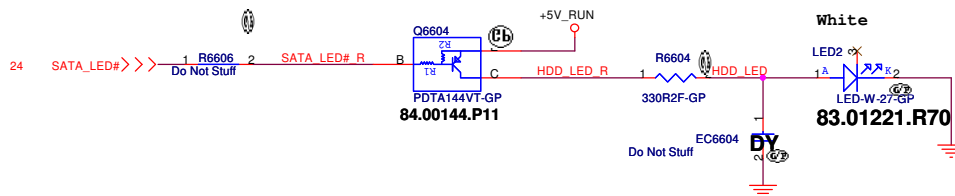
POWER LED



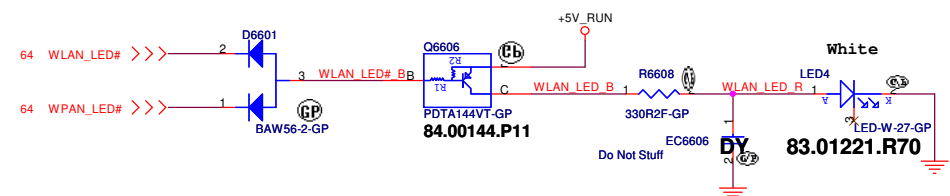
Battery LED



HDD LED



WLAN LED



DV15 CP UMA second

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Title			LED	
Size	Document Number	Rev		
A3	Enrico/Caruso 15 CP	A00		
Date:	Wednesday, April 13, 2011	Sheet	66	of 99

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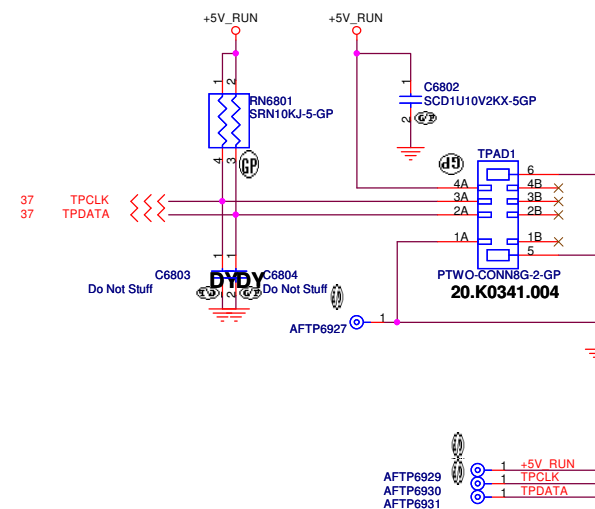


The diagram shows the pinout for the ACES-CON30-10-GP connector, which is a 32-pin connector. The pins are numbered 1 through 32. The connections are as follows:

- Pin 1: Connected to KB1 pin 31 and AFTP6901 pin 1.
- Pin 2: Connected to KROW7 pin 1 and AFTP6902 pin 1.
- Pin 3: Connected to KROW6 pin 1 and AFTP6903 pin 1.
- Pin 4: Connected to KROW4 pin 1 and AFTP6904 pin 1.
- Pin 5: Connected to KROW2 pin 1 and AFTP6905 pin 1.
- Pin 6: Connected to KROW5 pin 1 and AFTP6906 pin 1.
- Pin 7: Connected to KROW1 pin 1 and AFTP6907 pin 1.
- Pin 8: Connected to KROW3 pin 1 and AFTP6908 pin 1.
- Pin 9: Connected to KROW0 pin 1 and AFTP6909 pin 1.
- Pin 10: Connected to KCOL5 pin 1 and AFTP6910 pin 1.
- Pin 11: Connected to KCOL4 pin 1 and AFTP6911 pin 1.
- Pin 12: Connected to KCOL7 pin 1 and AFTP6912 pin 1.
- Pin 13: Connected to KCOL6 pin 1 and AFTP6913 pin 1.
- Pin 14: Connected to KCOL8 pin 1 and AFTP6914 pin 1.
- Pin 15: Connected to KCOL3 pin 1 and AFTP6915 pin 1.
- Pin 16: Connected to KCOL1 pin 1 and AFTP6916 pin 1.
- Pin 17: Connected to KCOL2 pin 1 and AFTP6917 pin 1.
- Pin 18: Connected to KCOL0 pin 1 and AFTP6918 pin 1.
- Pin 19: Connected to KCOL12 pin 1 and AFTP6919 pin 1.
- Pin 20: Connected to KCOL16 pin 1 and AFTP6920 pin 1.
- Pin 21: Connected to KCOL15 pin 1 and AFTP6921 pin 1.
- Pin 22: Connected to KCOL13 pin 1 and AFTP6922 pin 1.
- Pin 23: Connected to KCOL14 pin 1 and AFTP6923 pin 1.
- Pin 24: Connected to KCOL9 pin 1 and AFTP6923 pin 1.
- Pin 25: Connected to KCOL11 pin 1 and AFTP6925 pin 1.
- Pin 26: Connected to KCOL10 pin 1 and AFTP6926 pin 1.
- Pin 27: Connected to CAP_LED R pin 1 and AFTP6932 pin 1.
- Pin 28: Connected to AFTP6919 pin 1.
- Pin 29: Connected to AFTP6921 pin 1.
- Pin 30: Connected to AFTP6922 pin 1.
- Pin 31: Connected to AFTP6923 pin 1.
- Pin 32: Connected to AFTP6925 pin 1.

The diagram also shows the following components and connections:

- KB1: A 32-pin connector with pins 1 through 32.
- KB_DET# 37: A signal line connected to pin 37 of the KB1 connector.
- ACES-CON30-10-GP: The main connector, with pins 1 through 32.
- 20.K0592.030: A component connected to pin 32 of the ACES-CON30-10-GP connector.
- AFTP6901 through AFTP6932: A series of components connected to pins 1 through 32 of the ACES-CON30-10-GP connector.
- Capacitor: A capacitor connected to pin 27 of the ACES-CON30-10-GP connector.
- Ground: A ground connection at the bottom of the diagram.



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Title

Hall Sensor

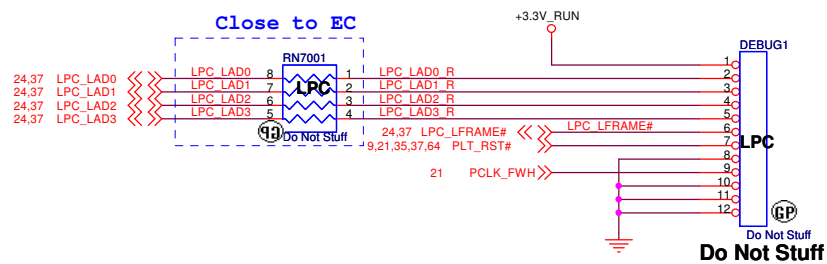
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Document Number
Enrico/Caruso 15 CP

Rev
A00

Date: Friday, April 08, 2011

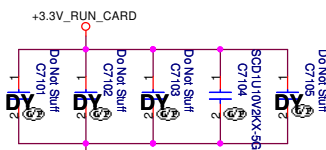
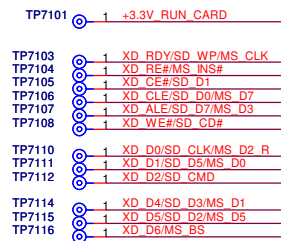
Sheet 69 of 99



DV15 CP UMA second

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Title			
Reserved			
Size A3	Document Number Enrico/Caruso 15 CP	Rev A00	
Date: Wednesday, April 13, 2011	Sheet 70 of 99		

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Sheet 72 of 99

DV15 CP UMA second



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	

Reserved

Size
A3

Document Number
Enr

Enrico/Caruso 15 CP


Rev
A00

Date: Friday, April 08, 2011

Sheet 73 of 99

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DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
A3	Enrico/Caruso 15 CP	A00
Date:	Friday, April 08, 2011	Sheet 74 of 99

(Blanking)

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Enrico/Caruso 15 CP

Rev
A00

Date: Friday, April 08, 2011

Sheet 75 of 99



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	A3
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Document Number **Enric**

Client Number **Enrico/Caruso 15 CP**

Rev
A00

Sheet	77	of	99
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	
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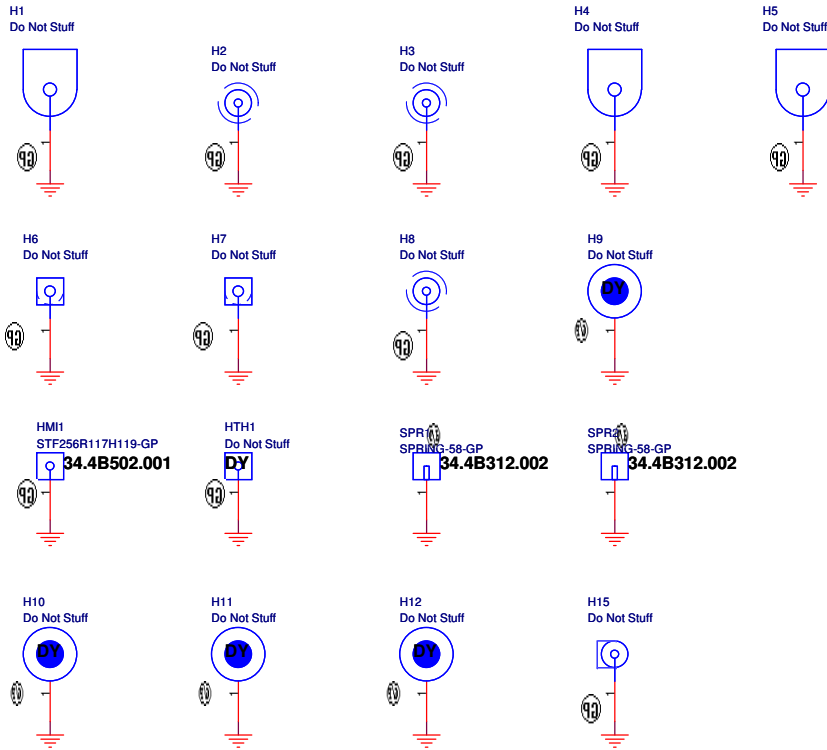
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Enrico/Caruso 15 CP

Rev

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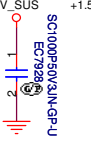
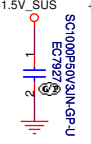
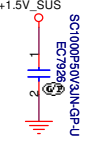
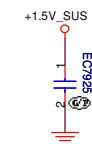
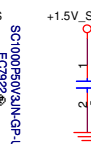
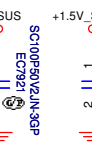
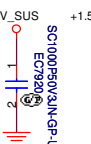
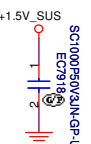
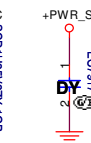
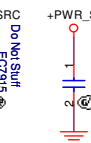
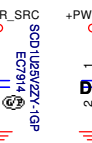
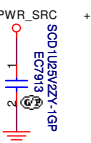
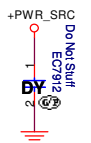
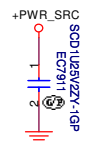
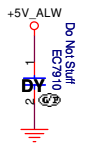
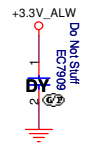
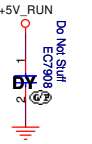
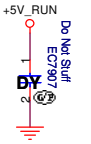
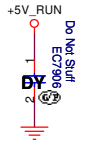
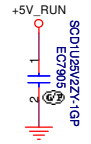
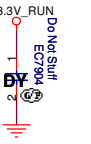
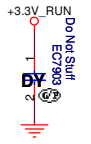
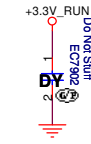
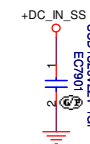


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STF256R117H119-GP
34.4B502.001

HTH1
Do Not Stuff
DY

SPR1
SPRING-58-GP
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SPR2
SPRING-58-GP
34.4B312.002



DV15 CP UMA second


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		Title UNUSED PARTS/EMI Capacitors	
Size A3	Document Number Enrico/Caruso 15 CP	Rev A00	
Date: Friday, April 08, 2011	Sheet 79 of 99		

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DV15 CP UMA second

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A3	Document Number Enrico/Caruso 15 CP		Rev A00
Date: Friday, April 08, 2011		Sheet 80 of 99	

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Neihu,
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Title

SizeA2

Document Number

Rev

Date: Friday, April 08, 2011


Sheet 82 of 99

Reserved

Enrico/Caruso 15 CP

A00

DV15 CP UMA second



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

Custom


Enrico/Caruso 15 CP

A00

Date: Friday, April 08, 2011

Sheet 84 of 99

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

Custom

Reserved
Enrico/Caruso 15 CP

A00

Date: Friday, April 08, 2011

Sheet 85 of 99



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

Reserved

Size
A3

Document Number

Enrico/Caruso 15 CP

Rev
A00

DV15 CP UMA second



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	Title
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Reserved

Size
A3

Document Number	
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Enrico/Caruso 15 CP

Rev
400

Date: Friday, April 08, 2011

Sheet 87 of 99

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,
Taipen Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
C

Document Number
Enrico/Caruso 15 CP

Rev
A00

Date: Friday, April 06, 2011

Sheet 88 of 99

DV15 CP UMA second



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
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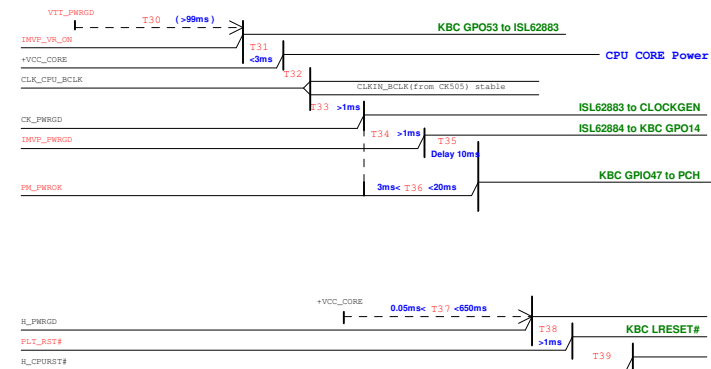
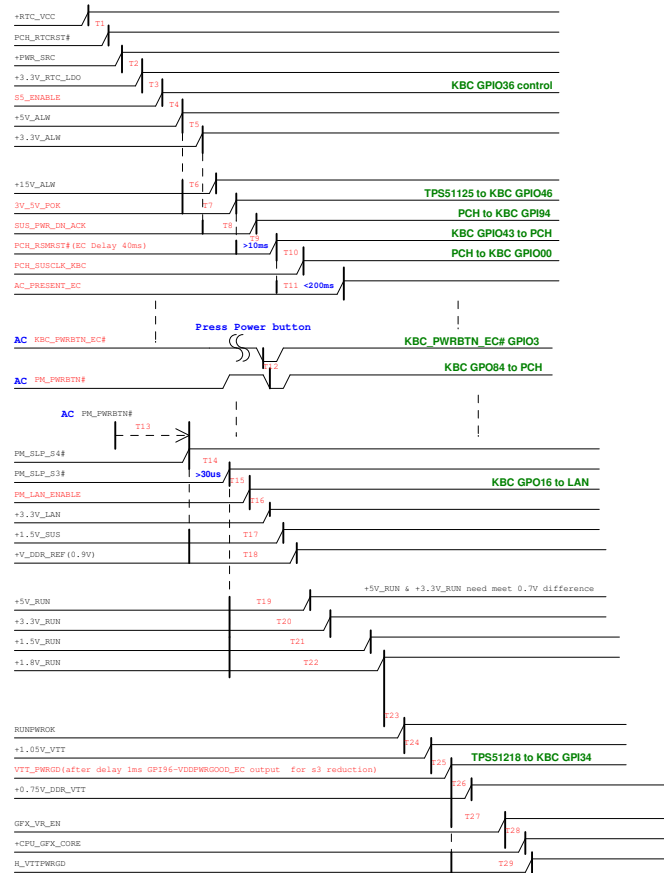
Rev
A00

Date: Friday, April 08, 2011

Sheet	89	of	99
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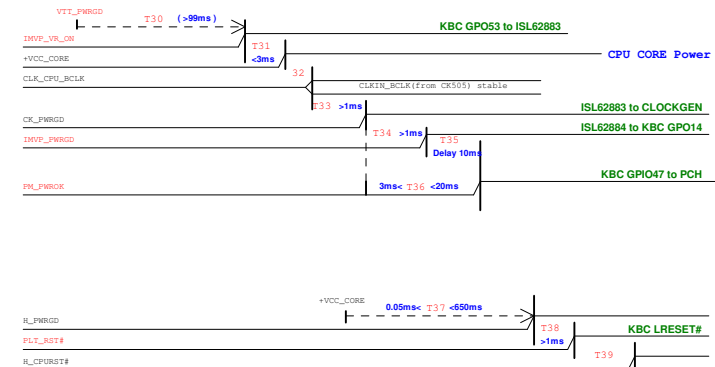
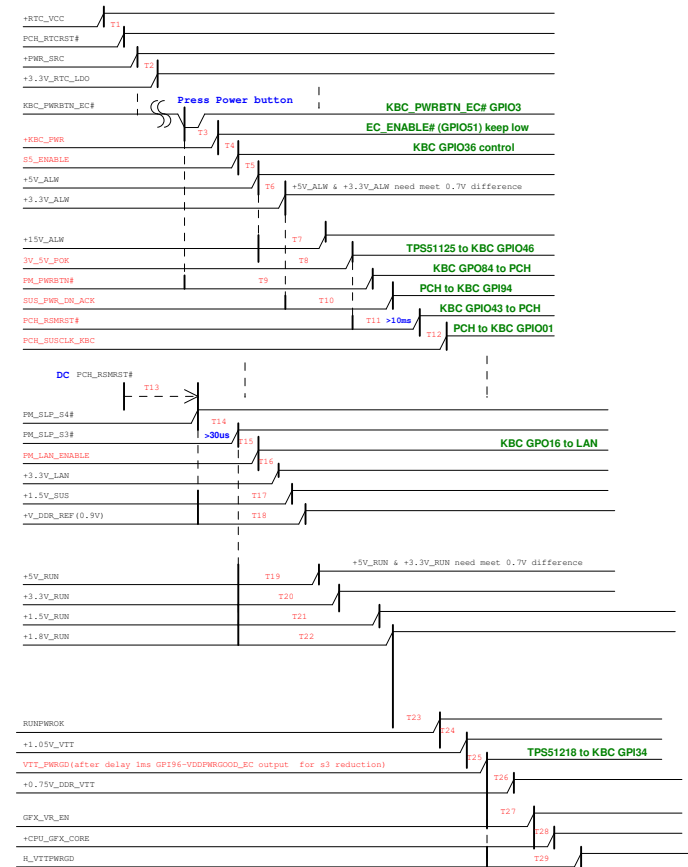
DV15 Calpepla UMA-Power Up Sequence (AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



Item	Pg.	Date	Description	Owner
KBC	37	A00-0412	stuff R3722 and DY R3725 for change MB version from X02 to A00	EE
WLAN	64	A00-0412	change R6415 from short pad to 0 ohm for debug	EE
USB	54, 63	A00-0412	Remove colay pad(R5403,R5404,R6315,R6316,R6317,R6318,R6319,R6320) after A00	EMI
USB	32, 64	A00-0412	Remove colay pad(EL3201,EL6401) and short pad(R3204,R3205,R6401,R6402) after A00	EMI
CLK GEN	7	A00-0412	change R710~R717 from 0 ohm to short pad	EMI
HDMI	57	A00-0412	Remove colay pad(EL5701,EL5702,EL5703,EL5704) after A00	EMI
short pad	ALL	A00-0412	change PR4519,PR5006,PR5111,R3202,R3742,R3743,R3744,R7105 from 0 ohm to short pad	EE
RTC	62	A00-0412	change U6203 P/N to 83.R0304.B81 for RTC detect leakage issue	EE
RT8237A_+1.05V	49	A00-0412	update PU4901 symbol for part manager footprint change	POWER
WLAN	64	A00-0412	add and DY R6416 0 ohm for Wimax future	EE
POWER GAP	ALL	A00-0413	change power GAP (PG4511,PG4602,PG4604,PG4605,PG4606,PG4615,PG4617,PG4619,PG4621,PG4624,PG4625,PG4607,PG4608,PG4609,PG4622,PG4626,PG4627,PG4610,PG4611,PG4612,PG4613,PG4614,PG4616,PG4618,PG4620,PG4902,PG4903,PG4904,PG4905,PG4906,PG4908,PG4910,PG4911,PG4913,PG4915,PG4917,PG4919,PG4925,PG4926,PG4920,PG4927,PG4928,PG4929,PG4909,PG4901,PG4912,PG4914,PG4916,PG4918,PG5001,PG5012,PG5002,PG5003,PG5004,PG5008,PG5009,PG5010,PG5011,PG5013,PG5015,PG5016,PG5017,PG5104,PG5106,PG5301,PG5303,PG5305,PG5308,PG5311) P/N from ZZ.CON2d.XXX to ZZ.CLOSE.001 for PSE requests	POWER
Thermal	39	A00-0422	stuff R3904 to change T8 temperature setting for reliability test	EE

DV15 CP UMA second



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Title

Change History

Size
A3

Document Number

Enrico/Caruso 15 CP


Rev

A00

Date: Friday, April 22, 2011

Sheet 91 of 99

Item					Pg.					Date					Description															Owner				

DV15 CP UMA second				A	
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Size A3	Document Number <i>Enrico/Caruso 15 CP</i>				Rev <i>A00</i>
Date:	Friday, April 08, 2011		Sheet	93	of 99

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

Change History

Size
A3

Document Number	
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A3	Enrico/Caruso 15 CP	A00
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Date: Friday, April 08, 2011

Sheet 94 of 99

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	

Change History

Size
A3

	Document Number
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Enrico/Caruso 15 CP

Rev
A00

Date: Friday, April 08, 2011

Sheet 95 of 99

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	

Change History

Size	A3
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Doc A3	Document Number	Enrico/Caruso 15 CP	Fig. A00
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Date: Friday, April 08, 2011

Sheet 96 of 99

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size
A3

Document Number	
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Enrico/Caruso 15 CP

Rev
A00

Date: Friday, April 08, 2011

Sheet 97 of 99



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

No.	Title	Date	Remarks
1
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Change History

Size A3	Document Number Enrico/Caruso 15 CP	Rev A00
Date: Friday, April 08, 2011	Sheet 98 of 99	

DV15 CP UMA second



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size
A3

Document Number	
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Enrico/Caruso 15 CP

Rev

A00

Date: Friday, April 08, 2011

Sheet	99	of	99
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